

Model 363 Channel Express Dual Receiver 14/400 Hardware Reference Manual



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1.0 Introduction

1.1 Contents and Structure

This manual describes the Model 363 Channel Express hardware and in conjunction with the items listed in the supporting documents of section 1.2 provides a complete description of the capabilities and operation of this product. The focus of this manual is the electrical function of the hardware including control structure, signal flow, clock distribution, external interfaces and key components. Other Channel Express manuals focus on software and the internals of the FPGA.

The manual is divided into nine sections as follows:

Section	Description
Section 1	Introductory information about the manual.
Section 2	Product overview.
Section 3	Hardware specifications.
Section 4	Absolute maximum conditions without damage.
Section 5	Hardware performance characteristics.
Section 6	Detailed hardware description.
Section 7	External interface descriptions and connector pinouts.
Section 8	Hardware build options
Section 9	Technical support

The latest product documentation and software is available for download from the Red Rapids web site (www.redrapids.com) by following the Technical Support link.

1.2 Supporting Documents


Author	Number	Title
Red Rapids	REF-360-001	Channel Express Installation Guide
Red Rapids	REF-360-002	Channel Express Software Reference Manual
Red Rapids	REF-360-003	Channel Express FPGA Core Manual
Red Rapids	DSK-820-013	Model 363 Power Calculator (Excel™)
ANSI/VITA	42.0-2005	XMC Switched Mezzanine Card Auxiliary Standard
ANSI/VITA	42.3-2006	XMC PCI Express Protocol Layer Standard
PCI SIG	PCI Express Base Rev 2.0	PCI-SIG, PCI Express Base Specification Revision 2.0

1.3 Conventions

This manual uses the following conventions:

- Hexadecimal numbers are prefixed by “0x” (e.g. 0x00058C).
- *Italic* font is used for names of registers.
- **Bold** font is used for names of directories, files and OS commands.
- Palatino font is used to designate source code.
- Active low signals are followed by ‘#’, For example, TRST#.

 Text in this format highlights useful or important information.

 Text shown in this format is a warning. It describes a situation that could potentially damage your equipment. Please read each warning carefully.

The following are some of the acronyms used in this manual.

- | | |
|---------------------|--|
| • ADC | Analog to Digital Converter |
| • API | Application Program Interface |
| • CMC | Common Mezzanine Card |
| • CPCI | CompactPCI |
| • DAC | Digital to Analog Converter |
| • DCM | Digital Clock Manager |
| • DMA | Direct Memory Access |
| • FRU | Field Replaceable Unit |
| • GPIO | General Purpose Input/Output |
| • IDELAY | Virtex Input Delay Element |
| • IDELAYCTRL | Virtex Input Delay Control Element |
| • IOB | Virtex Input/Output Block |
| • MSPS | Mega Samples per Second |
| • PCI | Peripheral Component Interconnect |
| • PMC | PCI Mezzanine Card |
| • QDR | Quad Data Rate |
| • SFDR | Spur Free Dynamic Range |
| • SINAD | Signal-to-Noise and Distortion |
| • SNR | Signal-to-Noise Ratio |
| • TCXO | Temperature Compensated Crystal Oscillator |
| • UCF | Virtex User Constraints File |

1.4 Manual Compatibility

The applicable hardware part numbers are defined as follows:

- Model 363-XXX⁽¹⁾ *Channel Express 14/400*

⁽¹⁾ XXX is a three digit number that indicates the hardware variant.

1.5 Revision History

Version	Date	Description
R00	11/26/08	Initial release.

2.0 Overview

The Channel Express product family provides the ideal platform to rapidly field application specific I/O functions minus the expense of custom hardware development. The architecture features a high performance front-end tightly coupled to a Xilinx Virtex-5 FPGA. The FPGA communicates directly with the host processor through the PCI Express interface. Simple interfaces to the ADC, I/O, SRAM and SDRAM are easily integrated with user application logic.

The Channel Express product family offers several different front-end hardware options. The Model 363, illustrated in Figure 2-1, provides a dual channel digitizer based on the Texas Instruments AD5474 14-bit/400Mps A/D converter (ADC).

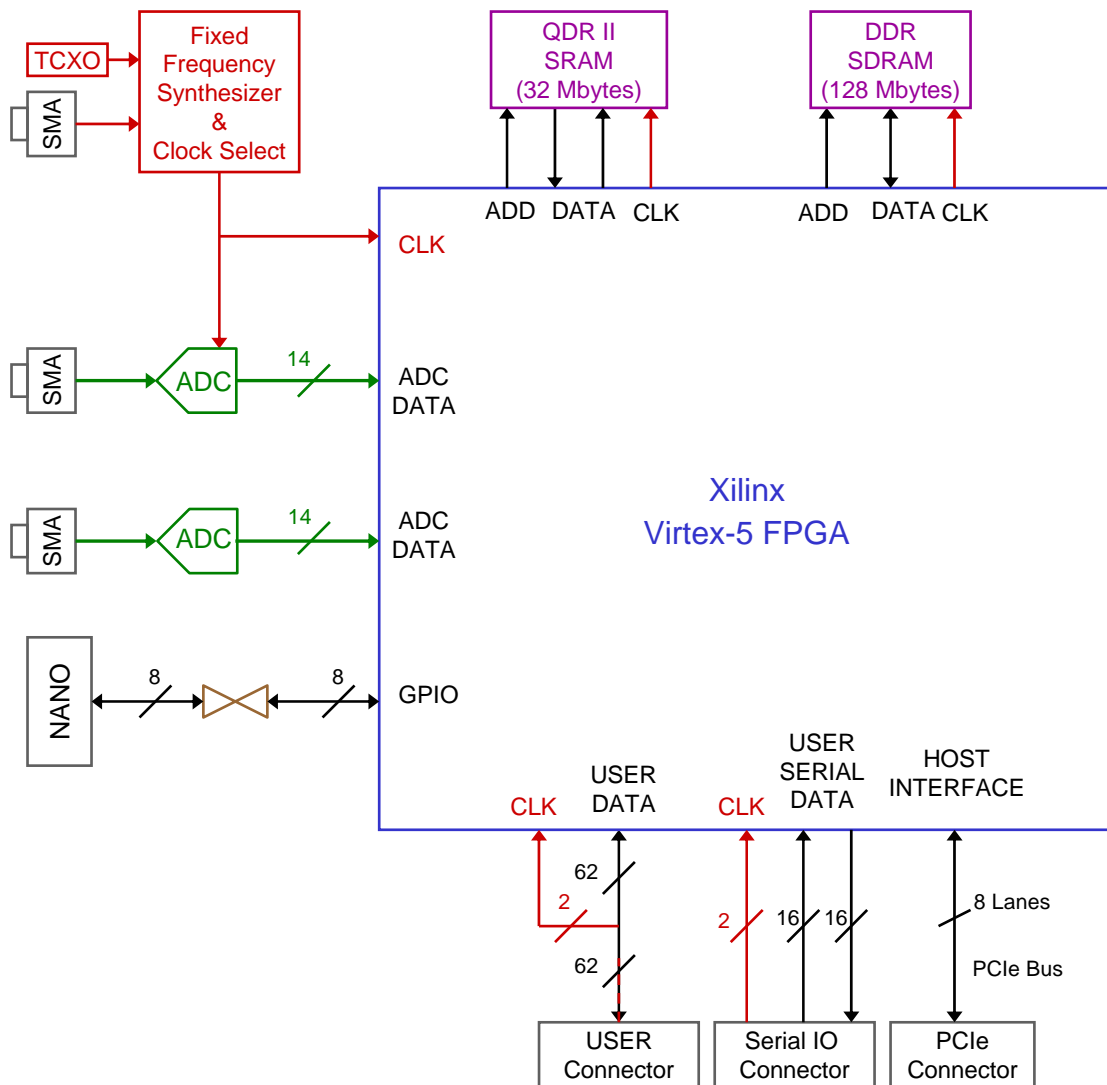


Figure 2-1 Model 363 Block Diagram

The AD5474 is a 14-bit digitizer with a 400 MHz sample rate and an analog signal input range of excess 1000 MHz. The ADC maintains good SNR and SFDR performance over a broad frequency range and is ideal for digitizing broadband signals.

The receiver sample clock is supplied by an on-board frequency synthesizer or an external source. The frequency synthesizer can be phase locked to the local 10 MHz temperature compensated crystal oscillator (TCXO) or an external reference can be used to achieve system-wide phase coherence.

The FPGA can be selected from the Virtex-5 high performance logic (LX) or signal processing (SX) platforms. A variety of size and speed grade options are offered to further optimize the price/performance ratio over a wide range of applications.

The FPGA can be connected to four optional 16-bit QDR SRAMs for high speed local data storage. The QDR SRAM provides separate read and write ports to maximize data transfer into and out of memory. This memory can also be used as a high-speed snapshot recorder to store segments of data without interruption from PCIe bus traffic. The FPGA can be also be connected to an optional 32-bit DDR SDRAM for additional local data storage.

An optional trigger input is provided to synchronize data collection to an external timing strobe. An additional high density connector supplies eight bidirectional lines for use as general purpose I/O.

Users also have access to two general IO ports connected directly from the FPGA to two external connectors. One IO port provides parallel access across 62 lines while the other provides high-speed serial access to the FPGA MGT interface over 8 differential transceiver pairs.

The host Interface implements the industry standard PCI express bus for high-speed communication between the host and card using up to 8 express lanes. The PCI Express standard is supported by a wide variety of host systems for data communication applications.

A DMA FPGA core is provided to manage data transfers between Channel Express and host memory. The DMA engine allows the receiver to automatically initiate a PCI burst transaction when a predetermined number of samples are available. An interrupt is generated by Channel Express when the specified number of data blocks have been written.

There are also more sophisticated DMA features built into the core. DMA chaining and scatter-gather techniques are supported by both the hardware and software to optimize data transfer efficiency. Refer to the product *Channel Express FPGA Core Manual* for further details.

The Virtex-5 FPGA is supported by a robust set of development tools from Xilinx. Creation of user configuration code follows the standard design flow using a pin assignment file supplied with Channel Express. VHDL source code for the ADC, SRAM and SDRAM are also provided. The configuration PROM can be programmed directly over the PCIe bus. The PROM and FPGA can be loaded through a JTAG connector using Xilinx iMPACT software.



The Channel Express product is intended for users with significant experience in FPGA design. As an alternative Red Rapids offers a line of fixed function products to meet standard data acquisition needs which require no FPGA design experience.

3.0 Hardware Specifications


All specifications estimated unless otherwise noted.


3.1 Board Specification Summary

Specification	Value
Physical	
XMC	VITA 42.0
Weight	3.8 ounces
Electrical	
Supply Voltages	3.3V, +12V, VPWR (+5V or +12V)
Bus Protocol	VITA 42.3 (PCI Express 1.0, Up to 8 Lanes)
Vendor ID (Hex)	0x17D2
Device ID (Hex)	0x00CA
Power (max) ⁽¹⁾	(see notes below)
Analog (AC-Coupled)	8.6 W (Not including digital)
Analog (DC-Coupled)	9.6 W (Not including digital)
Digital (No SRAM/SDRAM)	0.6 W (Not including FPGA)
Digital (32 MB SRAM)	10 W (Not including FPGA)
Digital (SDRAM)	0.85 W (Not including FPGA)
FPGA Core Current Limit	FPGA core current (1.0V) is limited to 12A
Environmental⁽²⁾	
Airflow (minimum)	250 LFM
Operating (Inlet Air)	
Temperature	0°C to 35°C Ambient
Humidity	90% maximum (non-condensing)
Altitude	15,000 Feet
Non-Operating	
Temperature	-20°C to 65°C Ambient
Humidity	95% maximum (non-condensing)
Altitude	40,000 Feet

⁽¹⁾The power dissipation of the FPGA is not included in section 3.1 since it depends on the specific application bitstream that is loaded. A power calculator spreadsheet is offered by Red Rapids to assist in the total power calculation for a specific application.

⁽²⁾The hardware has not been tested to the environmental specification listed in section 3.1.

 Download the Model 363 Power Calculator to determine the power requirements for your application.

 The maximum amount of FPGA core current (1.0V) supported by Channel Express is 12A.

3.2 Receiver Specifications


3.2.1 Receiver Input Levels

Parameter	Min	Typ	Max	Unit
Input Impedance		50		Ohms
ADC Offset Error ⁽¹⁾	-11		+11	mV
Un-calibrated DC Coupling Offset Error ⁽²⁾	-50		+50	mV
ADC Gain Error	-5%		+5%	FS
Full Scale Input (0 dBFS, 50 ohms)				
AC-Coupled Mode				
Input Voltage		2.5		V _{pp}
Input Power		+12		dBm
DC-Coupled Mode (TBD Gain)				
Common Mode Voltage Range		TBD		V
Input Voltage		TBD		V _{pp}
Input Power		TBD		dBm

Notes: ⁽¹⁾ ADC offset dominates when AC coupled

⁽²⁾ Typical DC offset due to component tolerance, does not include system DC variation.

3.2.2 Receiver Performance

 Performance may vary depending on the quality of the power supply and EMI environment of the host..

3.2.2.1 AC-Coupled Performance

Measurement conditions: T = 25°C, Supply Voltages (+12, -12, 5, 3.3) nominal

Parameter	Min	Typ	Max	Unit
Passband ⁽¹⁾				
1 dB	1		500	MHz
3 dB	0.1		1300	MHz
SNR ⁽⁴⁾				
20.17 MHz Input ⁽²⁾		70.4		dB
70.17 MHz Input ⁽²⁾		70.3		dB
125.17 MHz Input ⁽³⁾		70.0		dB
SINAD ⁽⁴⁾				
20.17 MHz Input ⁽²⁾		70.2		dB
70.17 MHz Input ⁽²⁾		70.1		dB
125.17 MHz Input ⁽³⁾		69.8		dB
SFDR				
20.17 MHz Input ⁽²⁾		86		dB
70.17 MHz Input ⁽²⁾		84		dB
125.17 MHz Input ⁽³⁾		84		dB
Channel to Channel Isolation				
50 MHz		>90		dB
250 MHz		85		dB
500 MHz		80		dB
1000 MHz		70		dB

Notes:

⁽¹⁾ Measured across band using ADC output.

⁽²⁾ Measured with a 400 MHz external sample clock.

⁽³⁾ Measured with a 400 MHz external sample clock. Performance extrapolated from -4 dBFS plot due to test equipment limitations.

⁽⁴⁾ Derived from -10dBFS measurements due to test equipment limitations.

3.2.2.2 DC-Coupled Performance (TBD)

3.3 External Reference/Clock/Trigger Input Levels

Parameter	Min	Typ	Max	Unit
External Reference (REF)				
Input Impedance		50		Ohms
Input Voltage (50 Ohms)	1.5		3.5	V _{pp}
Input Power (50 Ohms)	+7		+14.8	dBm
Frequency	10		10	MHz
External Clock Input (CLK IN)				
Input Impedance		50		Ohms
Input Voltage (50 Ohms)	0.8	2.8	2.8	V _{pp}
Input Power ⁽¹⁾ (50 Ohms)	+2	+13	+13	dBm
Frequency	236 ⁽²⁾		400	MHz
Trigger Input (TRIG)				
Input Impedance		50		Ohms
VIL	-0.5		0.8	V
VIH	2.4		5.5	V

Notes: ⁽¹⁾ See external clock discussion on square vs. sine input.

⁽²⁾ Minimum DCM setting for Diagnostic program, User may change the DCM setting to values as low as 50MHz.

3.4 Internal Clock Performance

Parameter	Min	Typ	Max	Unit
Internal Sample Clock				
Frequency (default)		400		MHz
Reference Spurs			75	dBc
Phase Noise				
1 kHz offset		-90		dBc/Hz
10 kHz offset		-100		dBc/Hz
100 kHz offset		-120		dBc/Hz
Internal Reference				
Frequency (default)		10		MHz
Stability	-1.0		+1.0	ppm
Phase Noise				
1 kHz offset		-125		dBc/Hz
10 kHz offset		-145		dBc/Hz
100 kHz offset		-148		dBc/Hz

3.5 USER IO Voltage Levels

The table below provides voltage levels for LVTTL modes of operation. Due to the wide variety of IO standards supported by direct connection to the FPGA, users should refer to the FPGA data sheet for voltage level information for non LVTTL modes.

Parameter	Min	Typ	Max	Unit
3.3V LVTTL				
VIH	2.0		3.45	V
VIL	-0.2		0.8	V
VOH	2.4			V
VOL			0.4	V
IIN		+/-5		uA
IOH at VOH ⁽¹⁾	-24			mA
IOL at VOL ⁽¹⁾			24	mA

⁽¹⁾Current determined by FPGA drive strength setting.

3.6 GPIO Voltage Levels

The table below provides voltage levels for LVTTL modes of operation. Due to the wide variety of IO standards supported by direct connection to the FPGA, users should refer to the FPGA data sheet for voltage level information for non LVTTL modes.

Parameter	Min	Typ	Max	Unit
3.3VLVTTL				
Input Impedance		10k		Ohms
VIH (with buffer)	2.0		5.5	V
VIH (without buffer)	2.0		3.45	V
VIL	-0.2		0.8	V
VOH	2.4			V
VOL			0.4	V
IOH at VOH ⁽¹⁾	-24			mA
IOL at VOL ⁽¹⁾			24	mA
3.3V Aux Power Option				
Voltage Output	3.1	3.3	3.5	V
Current			0.5	A

⁽¹⁾Current determined by FPGA drive strength setting.

4.0 Absolute Maximum Specifications

Stresses above those listed in Table 4-1 may cause damage to the unit. The operation of the unit at these or any other conditions outside of those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may degrade unit reliability.

Table 4-1 Absolute Maximum Specifications

Parameter	Min	Typ	Max	Unit
Environmental (Inlet Air)				
Operating Temperature	-30		50	C
Non-Operating Temperature	-30		85	C
Airflow	250			LFM
Receiver Inputs (50 Ohms)				
AC-Coupled				
DC Input Voltage	-10		10	V
AC Voltage Swing			4.4	V _{pp}
AC Input Power			+17	dBm
DC-Coupled				
DC Offset from Common		TBD		V
AC Voltage Swing		TBD		V _{pp}
AC Input Power		TBD		dBm
Reference Clock Input (50 Ohms)				
DC Level	-10		10	V
AC Swing			4.5	V _{pp}
AC Power			+17.5	dBm
Sample Clock Input (50 Ohms)				
DC Level	-10		10	V
AC Swing			4	V _{pp}
AC Power			+16	dBm
GPIO				
Buffered inputs	-0.5		5.0	V
Un-buffered inputs (Bypass)				
2.5V Power Rail	-0.5		2.8	V
3.3V Power Rail	-0.5		3.6	V
USER IO				
2.5 V IO Power Rail	-0.5		2.8	V
3.3 V IO Power Rail	-0.5		3.6	V



Exposure to absolute maximum conditions for extended periods may degrade unit reliability.

5.0 Typical Performance Characteristics

This section contains frequency response and spectral plots of the Model 363 hardware. These spectral plots provide an indication of receiver performance for a limited set of conditions. All of the data is measured with an external sample clock unless otherwise noted.

5.1 Receiver Performance

The following sections contain spectrum plots of the Model 363 receiver showing typical performance for a variety of sine wave inputs. The receiver performance section is divided into AC and DC coupled subsections. Each sine input is characterized using a 8192 point FFT. All data was collected with a 400 MHz sine external sample clock unless otherwise indicated.

5.1.1 AC-Coupled

The following receiver plots were taken with the Model 363 configured for the AC-coupled build option.

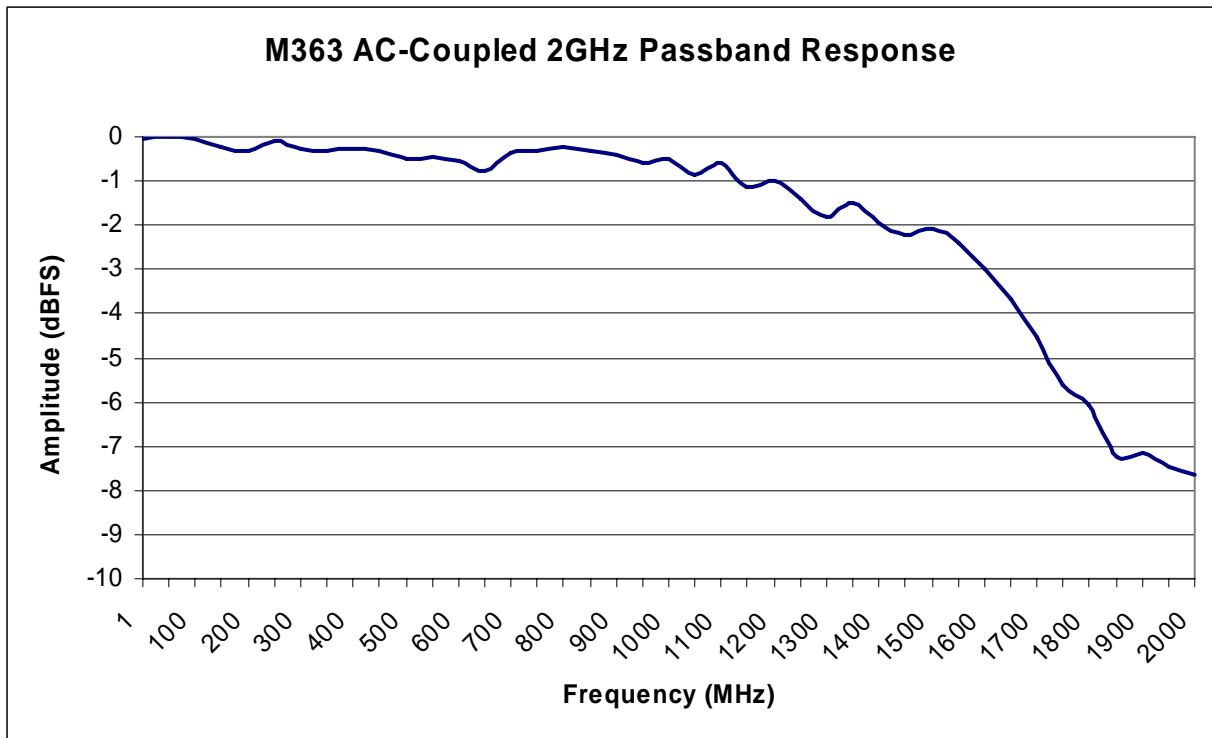


Figure 5-1 AC-Coupled Passband Profile 1 MHz to 2000 MHz

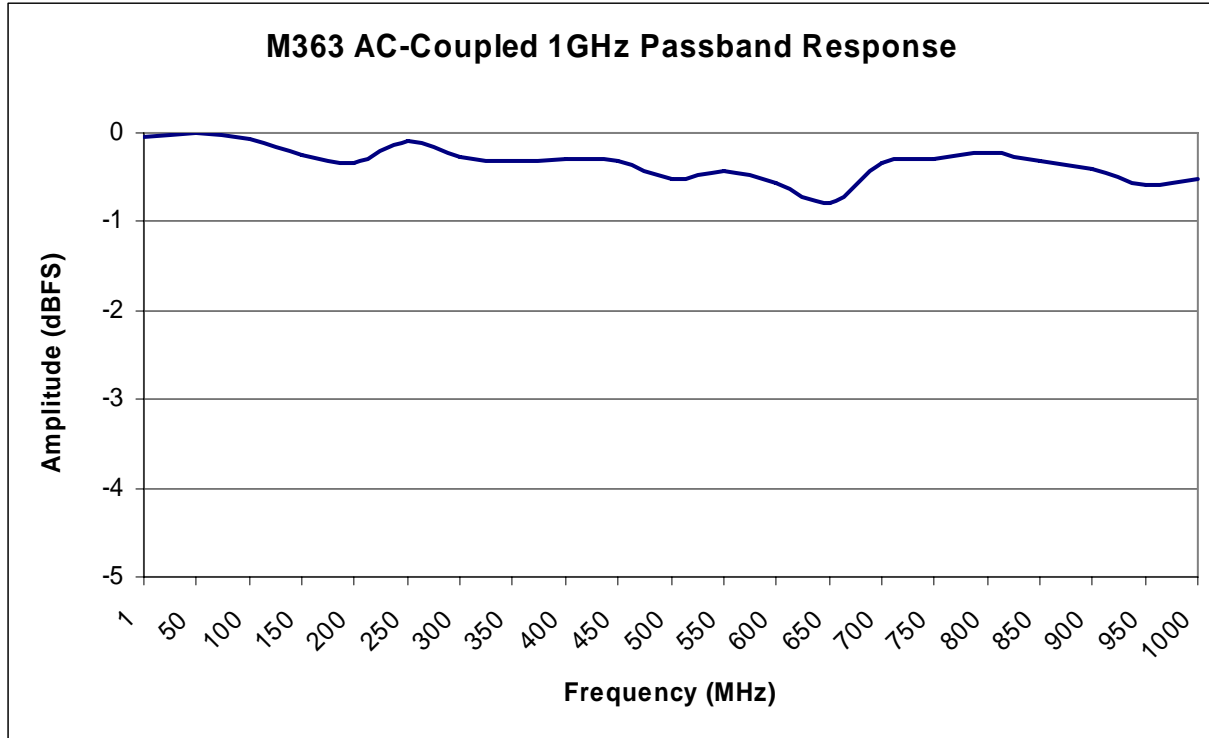


Figure 5-2 AC-Coupled Passband Profile 1 MHz to 1000 MHz

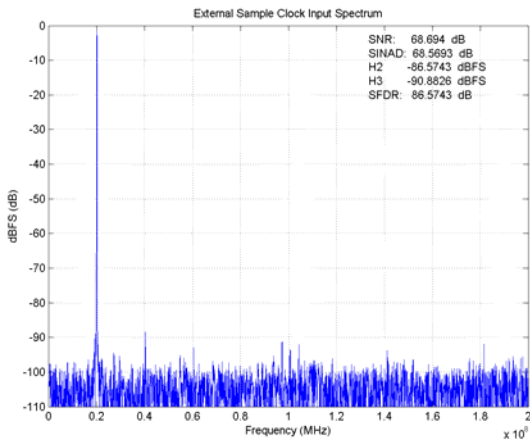


Figure 5-3 20.17354MHz, -1.6dBFS,

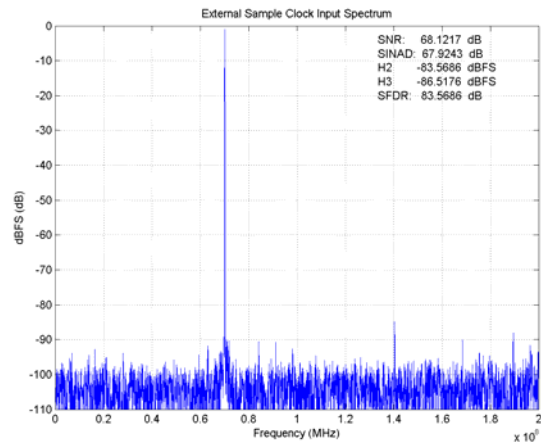


Figure 5-4 70.17543MHz, -1.2dBFS,

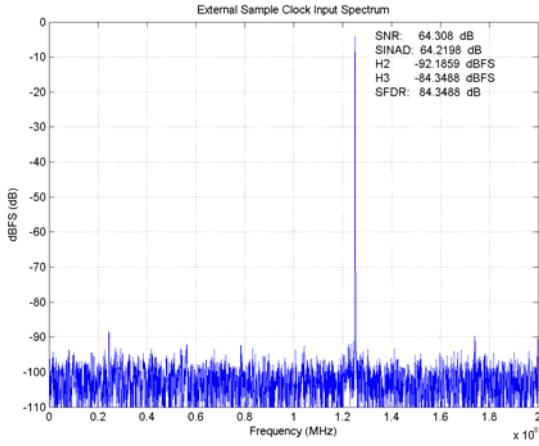


Figure 5-5 125.17543MHz, -4.0dBFS

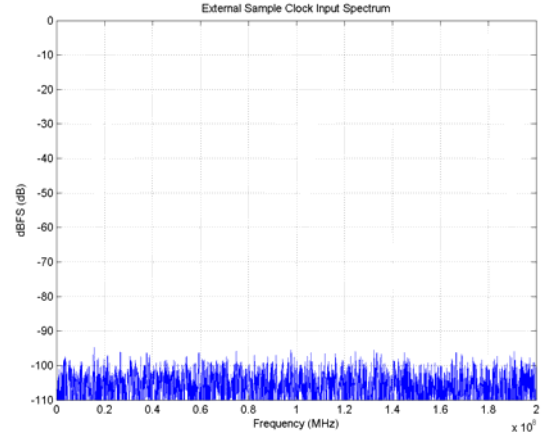


Figure 5-6 Terminated Input

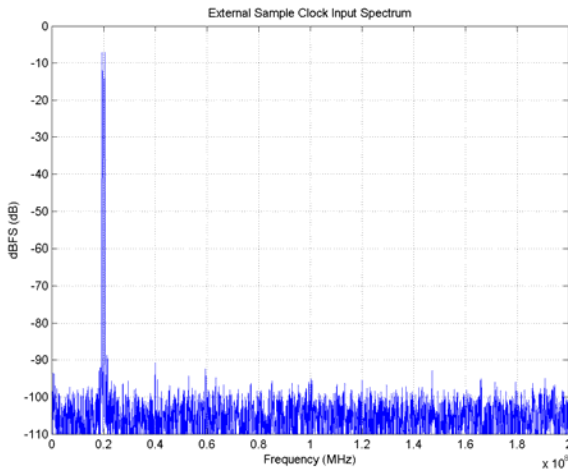


Figure 5-7 Two-tones 19.5 and 20.5 MHz at -7dBFS

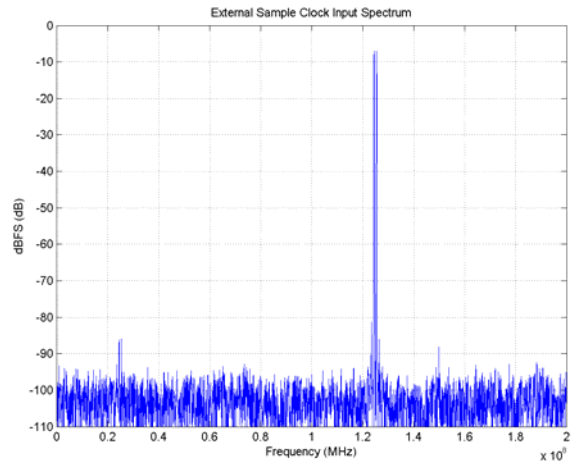


Figure 5-8 Two-tones 124.5 and 125.5 MHz at -7dBFS

5.1.2 DC-Coupled

DC-coupled characterization data is not available at this time.

5.2 Generating Characterization Plots

The wide dynamic range and input bandwidth characteristics of the Channel Express family levy strict signal conditioning requirements on test equipment used to characterize board performance. Even the highest quality general purpose RF signal generators output harmonics and noise that must be reduced in order to accurately characterize system performance. Generally a narrow bandpass filter is inserted between the signal generator output and the Channel Express receiver input. The bandpass filter should be as narrow as possible to eliminate generator harmonics and limit the amount of generator phase noise input into the receiver. Red Rapids' characterization plots were created using 5% bandwidth 7-section Chebyshev filters with > 55 dB of stop band rejection. We used filters from TTE such as their KC7t-70m-3.5m-50-720a. Table 5-1 contains a list of test equipment used to generate the characterization plots of section 5.0. The characterization frequency plots were generated by performing a 8k FFT on 8k data samples collected from the Channel Express receiver.

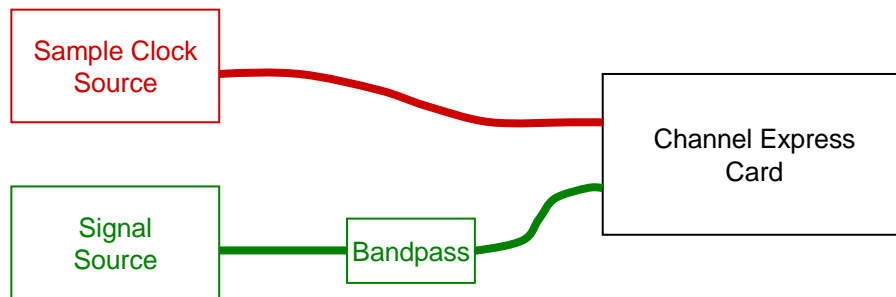


Figure 5-9 Characterization Setup


 Use a narrow bandpass filter between the signal generator and Channel Express card to accurately characterize system.

Table 5-1 Characterization Test Equipment

Function	Part Number	Manufacturer
Signal Generator	HP8648B	Agilent
Bandpass Filter	KC7t-70m-3.5m-50-720a	TTE
Sample Clock Generator	HP8648B	Agilent

6.0 Hardware Description

A high-level block diagram of the M363 Channel Express card is shown in Figure 6-1. The hardware description is divided into seven sections consisting of FPGA, receiver, sample clock distribution, SRAM, SDRAM, IO and key components. The following paragraphs provide a detailed description of each section.

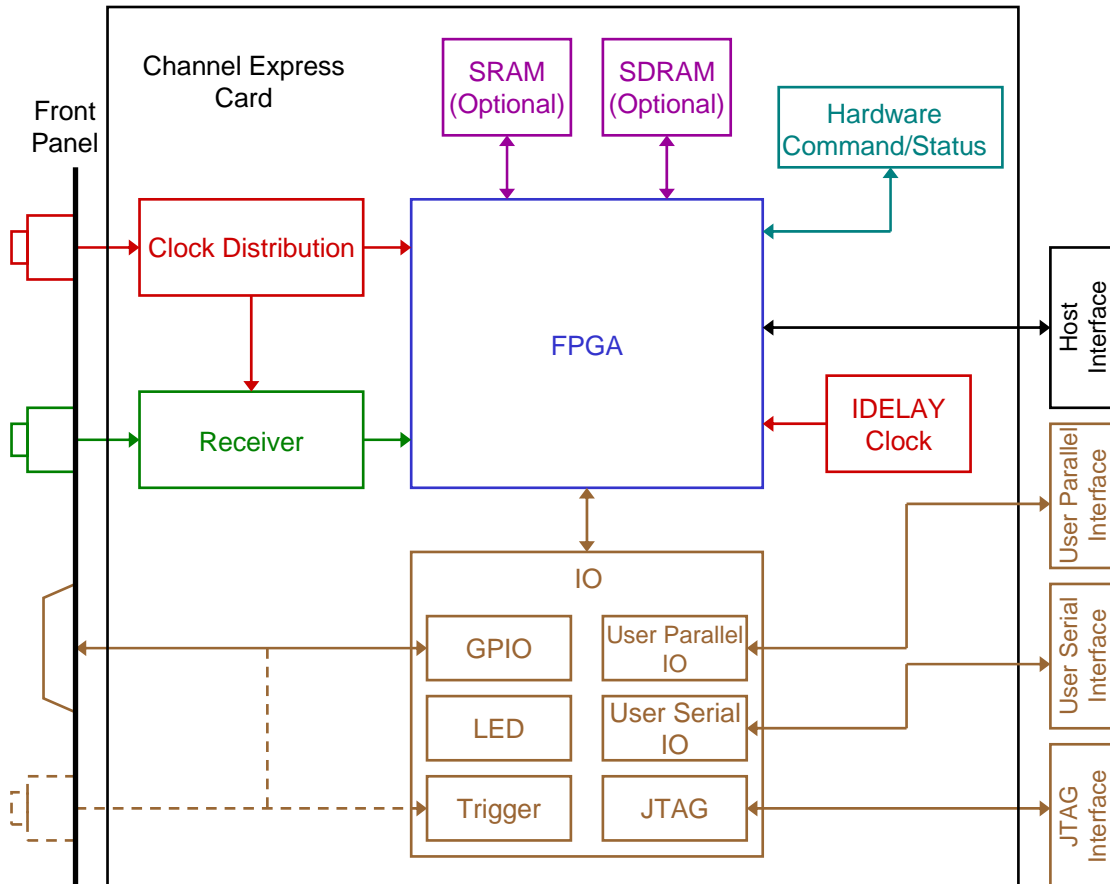


Figure 6-1 Model 363 Hardware Block Diagram

6.1 FPGA

A high-level block diagram of the FPGA with internal cores and interfaces is shown in Figure 6-2. Red Rapids provides FPGA cores to the SRAM, SDRAM, Receiver and Host Interface to ease integration of FPGA application code with the Channel Express hardware. The IO interfaces are governed by the FPGA User Constraints File (UCF) supplied along with the cores. An external 200 MHz oscillator is available as a source for IDELAY configuration within the FPGA.

The Channel Express FPGA support package includes VHDL source code for the ADC, SRAM, SDRAM and Host interface cores. Red Rapids also provides two FPGA diagnostic configurations in Xilinx Serial Vector Format (XSVF) to help verify the health of the Channel Express hardware. Details regarding the cores can be found in the *Channel Express FPGA Core Manual*. Diagnostic information can be found in the *Channel Express FPGA Software Manual*.

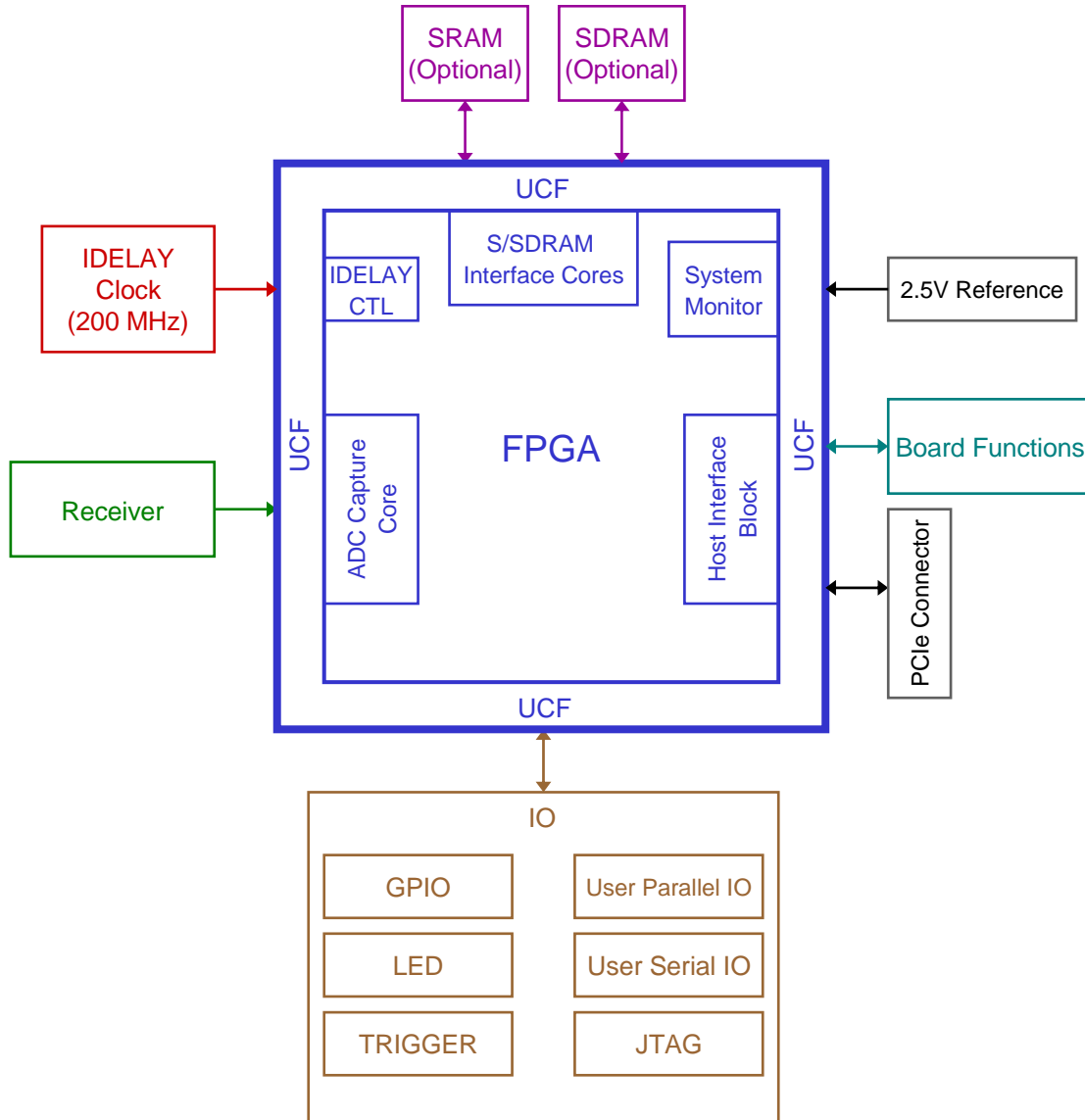


Figure 6-2 FPGA Cores and Interfaces

6.1.1 FPGA Cores and Functions

The following paragraphs describe some of the cores and functions available inside the FPGA.

6.1.1.1 ADC Capture Core

The ADC Capture core provides access to sample data produced by the digitizer. The clock input is supplied by a DCM core. A pre-configured DCM core is available for each Channel Express product to provide optimal clock settings for its ADC. This core is used in combination with registers located in the IOBs to capture ADC data.

6.1.1.2 SRAM Interface Core

The QDR SRAM Interface core simplifies user interaction with external memory by managing all of the critical timing. The core also includes autocalibration logic that

runs each time the hardware is reset. The autocalibration procedure adjusts the IDELAY elements that are resident in the IOB to compensate for path delays in the return signals from each SRAM.

6.1.1.3 SDRAM Interface Core

The SDRAM Interface core simplifies user interaction with external memory by managing all of the critical timing. The core interacts with IDELAY elements that are resident in the IOB to compensate for path delays in the interface to the SDRAM.

6.1.1.4 IDELAY Controller

The IDELAYCTRL primitive must be instantiated in every design. This primitive is part of the FPGA fabric and does not connect to any other logic. Refer to the Xilinx documentation for further information about using the IDELAYCTRL primitive in a design. The IDELAYCTRL requires a 200 MHz reference clock (idelay_clk) to operate. This clock is supplied by an oscillator on the card.

6.1.1.5 System Monitor

Every member of the Virtex-5 FPGA family contains a single System Monitor, located in the center of its die. The System Monitor function is built around a 10-bit, 200-kSPS ADC. The ADC is used to measure FPGA physical operating parameters like on-chip power supply voltages and die temperatures. External analog inputs allow the ADC to monitor the physical environment of the board or enclosure. System Monitor is fully functional on power up.

Red Rapids supports the built-in System Monitor feature of the Virtex-5 through the addition of an external precision 2.5V reference. The system monitor dedicated differential analog input has also been brought out on a pair of general purpose IO pins as shown in Figure 6-3. For more information on GPIO see section 6.6.1. Specific part information on the 2.5V reference can be found in the vendor sheet. Voltage reference part number can be found in section 6.7. Connector pin out information can be found in section 7.1.

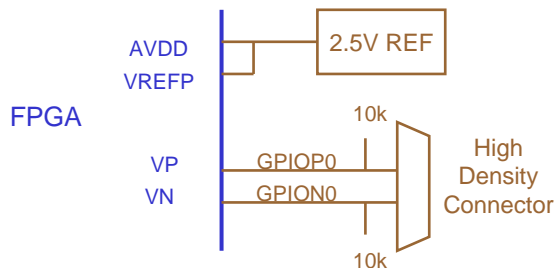



Figure 6-3 System Monitor Support

All System Monitor features are customizable at run time through the Dynamic Reconfiguration Port (DRP) and System Monitor control registers. These control registers can also be initialized at design time when System Monitor is instantiated in a design. For the latest information, including FAQs, software updates, and tutorials, refer to <http://www.xilinx.com/systemmonitor>.

 Please note that system monitor is a Xilinx primitive. Please refer system monitor support questions to Xilinx.

6.1.1.6 Host Interface Block

The Host Interface Block, shown in Figure 6-4, manages communication between the host and local bus connection within the FPGA. The block is organized into four user accessible cores designed to coordinate data, command and status transfers with the host.

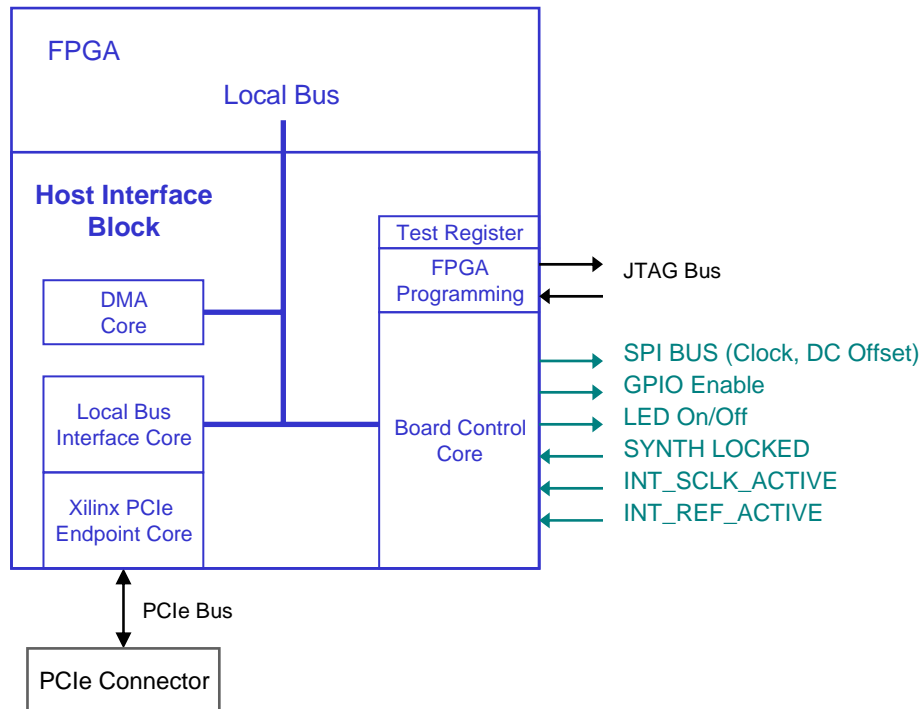


Figure 6-4 Host Interface Block Diagram

The primary host interface is implemented using the Xilinx PCIe Endpoint core. Red Rapids provides a Local Bus Interface core that converts the Endpoint core backside bus into a simple local bus format. The local bus is the primary communication conduit within the FPGA. The local bus connects to the DMA and Board Control cores as well as interfacing to user logic within the FPGA. The DMA core coordinates data transfer between the Channel Express card and host memory. The Board Control core consists of command/status registers that control various hardware functions on the card (ADC control, Clock Status, etc.). Details of the command register functions can be found in the *Channel Express Software Manual*. Source code is provided for the Local Bus, DMA and Board Control cores for more information please see the *Channel Express FPGA Core Reference Manual*.

The Host Interface block also facilitates host programming of the Configuration PROM over the PCIe Bus. User developed configuration files in Xilinx Serial Vector Format (XSVF) can be targeted to the Configuration PROM. For more information please see section 6.6.4 and the *Channel Express Software Manual*.

6.1.2 Host Interface Connector

The Host interface connector is defined by the ANSI/VITA XMC PCIe specification in terms of connector location and pin assignment. FPGA connections are listed in the UCF file found in the FPGA Development Kit download for the applicable Channel

Express card. A diagram showing board connectivity for ancillary signals is displayed in Figure 6-5. The diagram shows connections made to the on-board serial PROM, JTAG interface and FPGA reset.

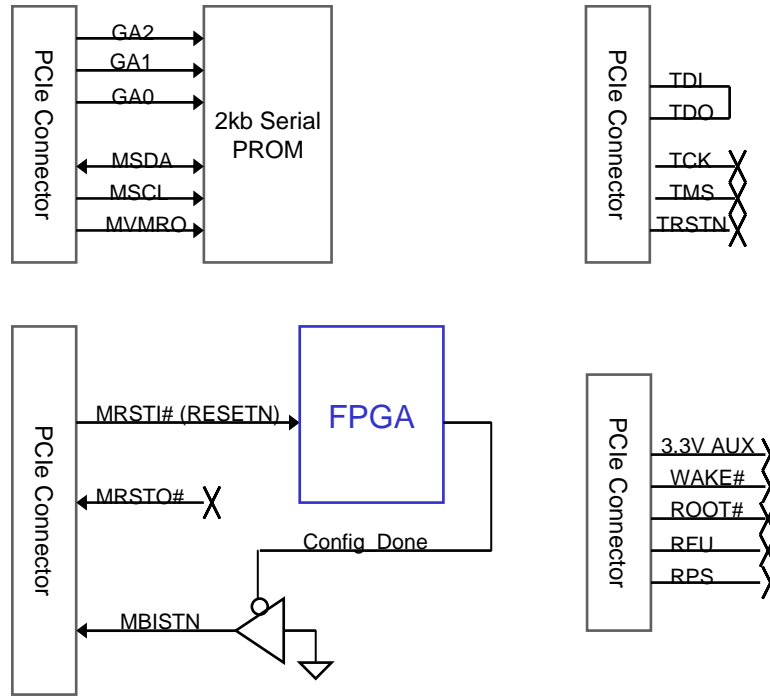


Figure 6-5 Host Interface Connection Detail

6.1.3 FPGA Build Options

The Channel Express Plus family provides for a wide selection of FPGA build options enabling the user to optimize their hardware for a variety of applications. The list of supported FPGA devices can be found in Table 6-1.

Table 6-1 Channel Express FPGA Options


Component	Part Number	Vendor	Comments
Virtex-5 FPGA	XC5VLX50T	Xilinx	Virtex-5 FPGA w/ Serial Links LX: High-performance logic SX: Ultra-high-performance DSP
	XC5VLX85T		
	XC5VLX110T		
	XC5VSX50T		
	XC5VSX95T		

6.1.4 FPGA Device Configuration

User configurations are developed using Xilinx standard design flow and tools. Once designs are compiled they can be loaded into the FPGA using one of two methods:

1. The FPGA can be loaded indirectly from a configuration PROM available for non-volatile storage of a bitstream that will load automatically at power-on.
2. The FPGA can be loaded directly through the JTAG connector using the Xilinx IMPACT software.

More information on JTAG programming can be found in section 6.6.4.



The FPGA cannot be directly programmed over the express bus interface since the endpoint core would be written over and lost to the host system during the process.

6.1.5 FPGA Power Utilization

The high performance capabilities of the Channel Express card can result in significant power consumption requirements and subsequent thermal considerations. This issue is of particular concern in units populated with high gate count FPGAs and large memory configurations. Unfortunately power consumption is a direct function of FPGA gate utilization, memory use and clock speed and thus highly application dependent. The following description is designed to provide the user with guidelines based on our analysis and customer experience to help provide some bounds to the problem.

The first step in the evaluation process is to estimate power consumption using Red Rapids power calculator spreadsheet in conjunction with the FPGA power estimation tool (a download from FPGA vendor) and values from section 3.1. Bear in mind that the results from the FPGA power estimation tool vary greatly with design assumptions. Once an initial estimate is made the power consumption requirement should be assessed in terms of the categories outlined in Table 6-2. This process should be repeated as the FPGA design is refined over time.

Table 6-2 Design Risk by Power Category

Power Consumption	Design Risk	Comments
<15 W	Low	Designs in this category have little or no thermal or supply issues as long as cooling air requirements are met.
15 -25 W	Med	Designs in this category should have detailed power estimation performed and system thermal management approach assessed.
>25 W	High	Designs in this category should look to reduce or offload processing and external memory usage. Designs will likely require added thermal management.

6.2 Receiver

A block diagram of the receiver is shown in Figure 6-6. The receiver consists of two independent analog channels labeled A and B. Each channel is accessed through an SMA connector and sampled by an ADC. The ADC sample clock is sourced by the clock distribution section. Each ADC output consists of a 14-bit data word and an overflow bit that connects to the FPGA. See the *Channel Express FPGA Core Manual* for more information on the ADC/FPGA interface.

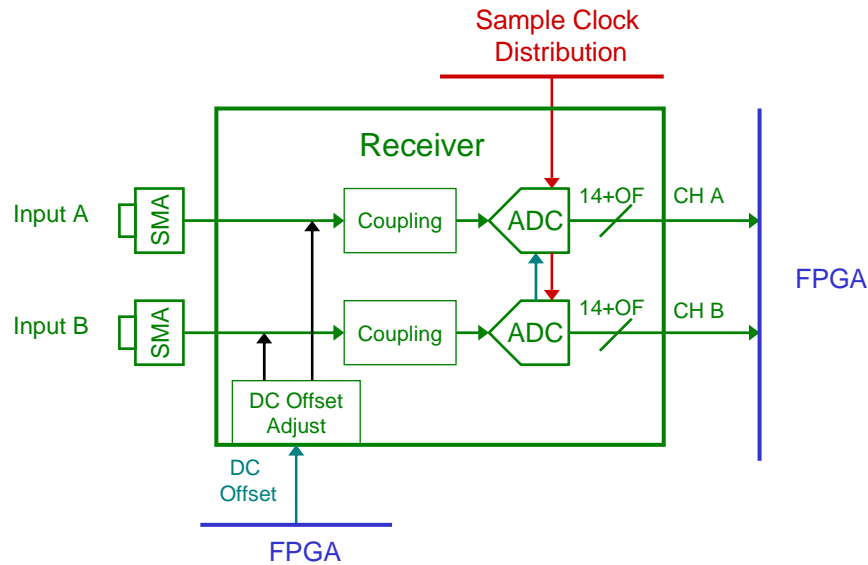


Figure 6-6 Receiver Block Diagram

6.2.1 Coupling and Offset Adjustment

The Model 363 receiver is available either AC or DC coupled as a build option. The AC-coupled option provides better high frequency dynamic performance at the expense of frequency response below 1 MHz and higher input drive levels. DC-coupling is performed using a differential amplifier which provides gain and frequency response down to DC. DC-coupled mode requires a dc-coupled system source impedance of 50 Ohms.



DC-coupled mode requires a dc-coupled source impedance of 50 Ohms.

The DC-coupled receiver option contains a set of DACs to trim DC offset errors as shown for a single channel in Figure 6-7. The DACs are arranged in pairs in a push-pull configuration. One DAC offsets the ADC input voltage in a positive direction while the other offsets the ADC input in a negative direction. DC offset adjustment is not available in AC-coupled mode. DC offset adjustment is accessed through the PCI Controller; more information is available in the *Channel Express Software Manual*.

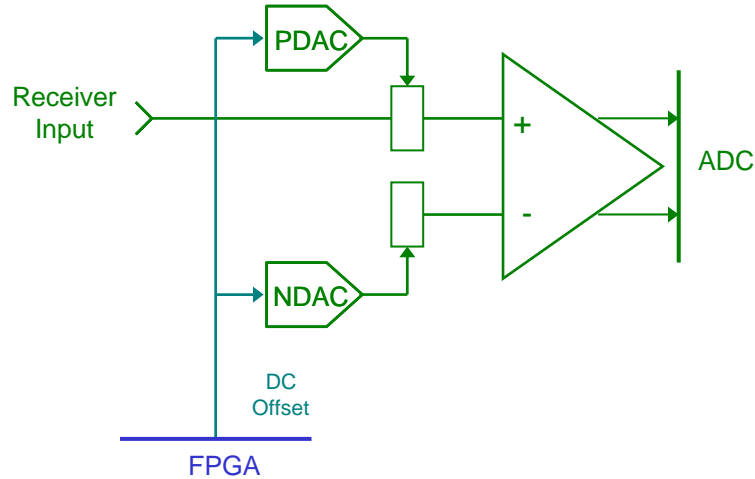



Figure 6-7 DC-Coupled Mode Offset Adjust

 Only one of the pair of offset DACs per input should be active at one time.

6.2.2 Hardware Configuration

The hardware configuration for each Model 363 ADC is summarized in Table 6-3. Receiver input levels are listed in the receiver interface description of section 3.2.1. Performance specifications can be found in section 3.2.2.

Table 6-3 Model 363 ADC Hardware Configuration

Item	Setting	Description
VCM	Decoupled	50 Ohm series with 0.1uF cap to ground
VREF	Decoupled	0.1uF cap to ground
Outputs	Terminated	All ADC outputs terminated inside FPGA
PDWN	RGND	2.0k Ohm resistor to ground.

6.3 Sample Clock Distribution

The board sample clock synchronizes the digitization and data movement functions of the Channel Express card. A block diagram of the Model 363 sample clock distribution system is shown in Figure 6-8. The clock can be sourced internally or externally and serves to time data acquisition into the FPGA as well as data transfer to RAM. The following paragraphs provide more detail on the clock distribution network.

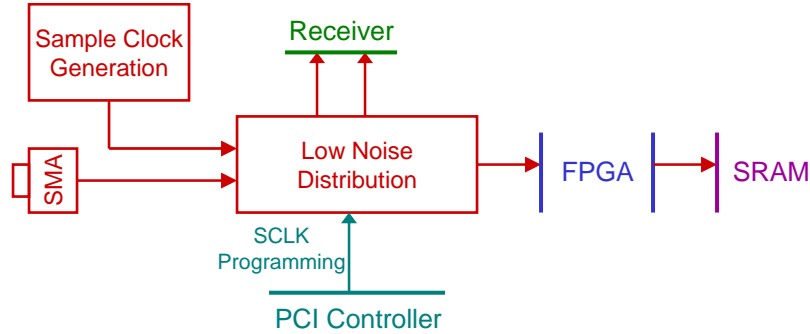


Figure 6-8 Model 363 Clock Distribution

6.3.1 Sample Clock Generator

The Model 363 sample clock may be generated from an on-board fixed frequency synthesizer or a user supplied external clock as shown in Figure 6-9. Power detectors are used to determine the presence of a sample clock or reference and notification is provided to the board control core.

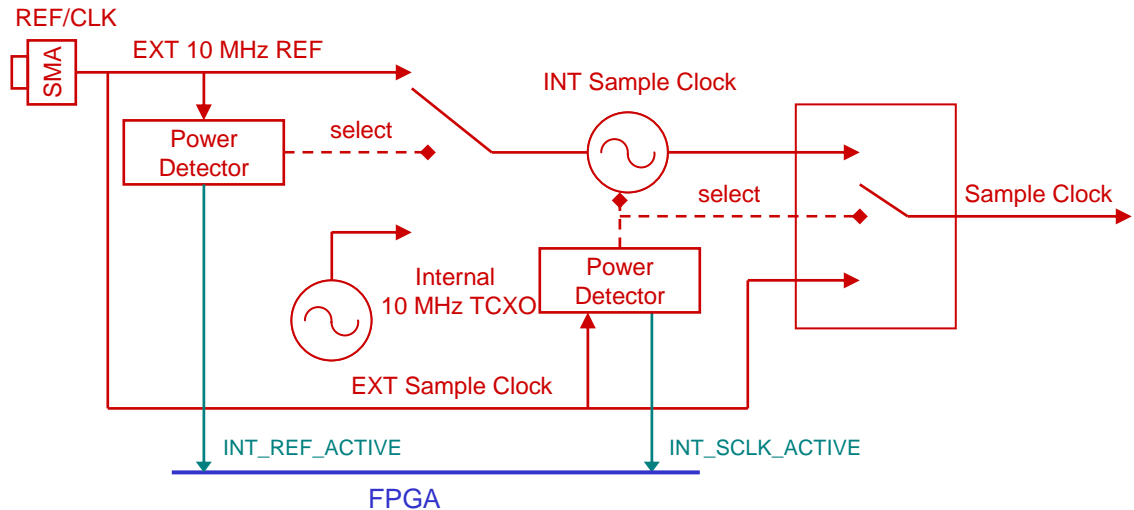




Figure 6-9 Sample Clock Generation


 The on-board synthesizer does not operate when an external sample clock is present.

6.3.1.1 External Sample Clock

An external sample clock signal is usually supplied by a high quality source that can provide good frequency stability ($< \pm 2$ ppm) and low phase noise (< 90 dBc/Hz @ 10 kHz, < 1 ps rms jitter). Quality RF Test equipment may be used as a sample clock source as long as it meets the Model 363 sample clock frequency and power requirements.


 The SNR of high frequency signals ($F_{in} > 100$ MHz) can be improved by using an external sample clock with better phase noise than that of the internal synthesizer.


The user supplied external clock waveform may be a sinusoid or square wave as long as the phase noise/jitter characteristic is low. Sine wave inputs should operate at the high end of the permissible input power range to maximize the voltage slope into the ADC clock circuitry. Square wave inputs may be driven at a lower power level since they already have a steep voltage slope.

 The user supplied external sample clock may be sinusoidal or square in nature so long as it possesses a low phase noise/jitter characteristic.

6.3.1.2 External Reference Clock

The on-board frequency synthesizer can be phase locked to an external 10 MHz system reference to achieve system-wide phase coherence by simply connecting a source to the reference/clock SMA. The AC power level on the reference input is continuously monitored to automatically detect the presence of an external source. If the power level exceeds the established threshold, the internal TCXO power is automatically turned off. There is hysteresis built into the detection circuit to prevent oscillation around the threshold. Only a high quality low phase noise (< -145 dBc/Hz @ 10 kHz) source should be used as an external reference. External reference source harmonic content above 50 MHz exceeding a level of -10dBm will cause the external clock detector to trip and supply the wrong sample clock. Clock input level requirements can be found in section 3.3.

 Generally the synthesized output of an RF signal generator should not be used as a 10 MHz reference source due to high phase noise. Most generators feature a separate dedicated low phase noise 10 MHz reference output that should be used instead.

 The spectral power level of the external reference source above 50 MHz must be less than -10dBm.

6.3.2 FPGA Clock Distribution

A copy of the sample clock is available to the FPGA from the low noise distribution chip. The low noise distribution clock is routed to a DCM within the FPGA and used to acquire data from each ADC and transfer data to the SRAM interface as shown in Figure 6-10. More information on the ADC and SRAM FPGA interface can be found in the *Channel Express FPGA Core Manual*

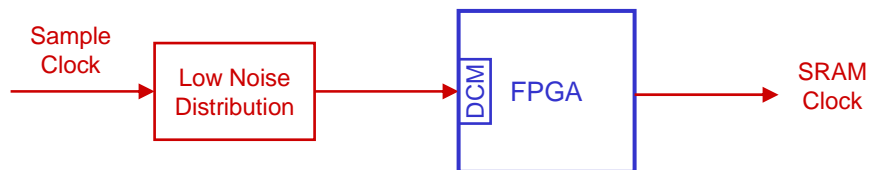


Figure 6-10 FPGA Clock Distribution

6.3.3 ADC Clock Distribution

A block diagram illustrating the data and clock paths for the receiver is shown in Figure 6-11. The ADC data from the receiver is registered into the FPGA using a copy of the sample clock. Data timing is controlled using an FPGA DCM as configured by the

ADC interface core. More information is available in the *Channel Express FPGA Core Manual*.

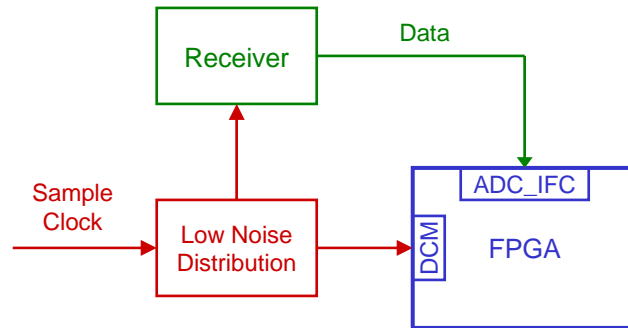


Figure 6-11 Receiver Data Clocking

6.4 SRAM (Build Option)

The Channel Express card can be ordered with an optional four banks of 250 MHz QDR II SRAM yielding an additional 32 Mbytes of storage external to the FPGA as shown in Figure 6-12. Each SRAM block represents a single QDR II SRAM device. The chip is organized as 4M x 18 bits, but only 16 bits of input and output are wired to the FPGA due to the limited number of pins available. The user interface to each SRAM is organized as 2M x 32 bits to ease the timing constraints on the application logic. More information about the SRAM can be found through the vendor data sheet associated with the device. Vendor name and device part number can be found in Table 6-4.

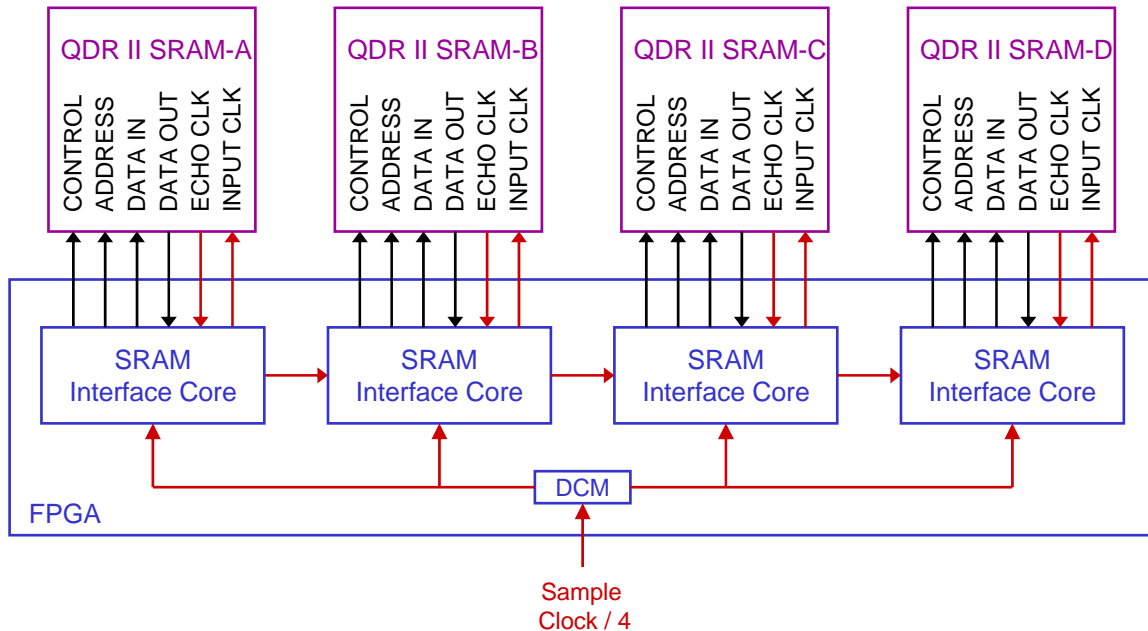


Figure 6-12 External SRAM Interconnect

The SRAM will not operate correctly if the input clock period is outside the range of 4.0 ns to 8.4 ns.

There is a delay-locked loop (DLL) internal to each SRAM that operates over a limited range of input frequencies (119 MHz to 250 MHz). A DCM inside the FPGA can multiply the sample clock to meet the SRAM frequency range requirement.

The Channel Express FPGA core library includes a DCM that automatically configures this device to the minimum allowable operating frequency greater than or equal to the ADC sample rate. However there may be some instances where the user may wish to operate at a higher legal multiple of the sample clock rate to process data.

The SRAM interface core in the FPGA manages the clock domain crossing between data collected at the sample rate and the SRAM running at an integer multiple of this value. Even if the sample and SRAM clock frequencies are matched, a single SRAM can continuously store data from two input channels since both the read and write ports operate at double data rate.

The SRAM interface FPGA core simplifies user interaction with the memory by managing all of the critical timing, including a self-calibration procedure that runs each time the hardware is reset. Please see the *Channel Express FPGA Core Manual* for more information.

6.5 SDRAM (Build Option)

The Channel Express card can be ordered with an optional single bank of 6ns DDR mobile SDRAM yielding an additional 128 Mbytes of storage external to the FPGA as shown in Figure 6-13. The chip is organized in 4 banks of 8M x 32 bits and standard size paging. More information about the SDRAM can be found through the Vendor data sheet associated with the device. Vendor name and device part number can be found in Table 6-4.

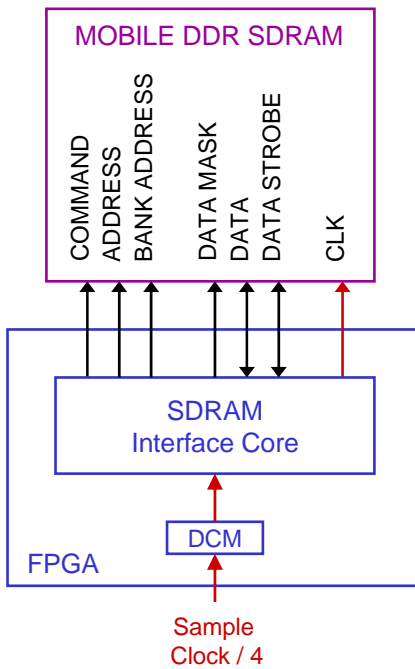


Figure 6-13 External SDRAM Interconnect

The SDRAM interface core in the FPGA manages the clock domain crossing between data collected at the sample rate and the SDRAM running at an integer multiple of this value. Please see the *Channel Express FPGA Core Manual* for more information.

6.6 IO

A block diagram of the Model 363 IO interface is shown in Figure 6-14. There are five user ports connected to the FPGA in addition to a number of LED indicators. The following paragraphs provide a summary of the IO functions found on the Model 363. IO connector details can be found in the external interface description of section 7.0.

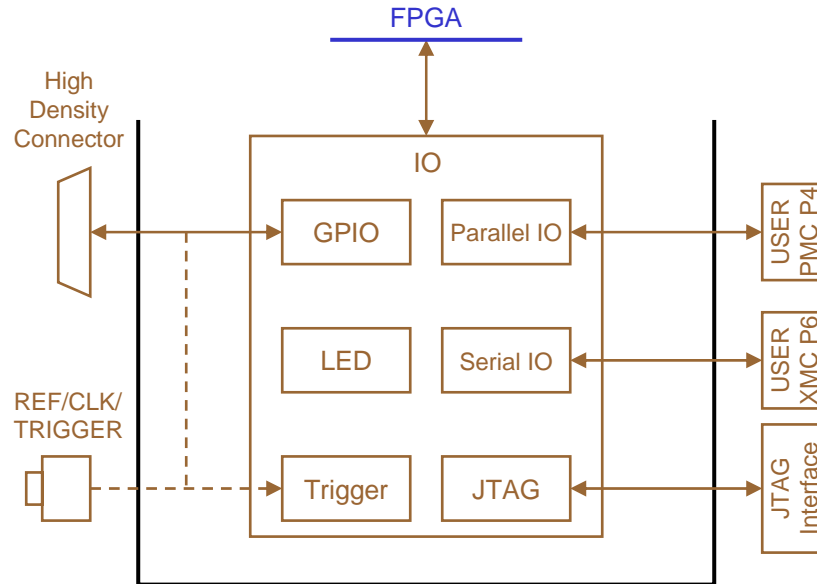


Figure 6-14 IO Block Diagram

6.6.1 GPIO Interface

The Model 363 includes a 15-pin high density front panel connector for general purpose I/O. There are 8 GPIO signals connected to pins on the FPGA as shown in Figure 6-15. The driver voltage (IO PWR) of the GPIO bank is tied to 3.3 V in standard configurations and can be tied to 2.5V as a build option.

The GPIO pins may use any of the FPGA protocols subject to the IOB and VCCO constraints listed in the Xilinx data sheet. See the FPGA data sheet for IO level and switching characteristics. FPGA part number information can be found in Table 6-4.


There are no terminations external to the FPGA, the only mechanism for termination are the built-in features of the Xilinx IOB. All lines are routed as 50 Ohm differential pairs and length matched to within 1 inch. The GPIO path contains a FET buffer to provide 5V tolerance and provide FPGA protection. The buffer may be bypassed with zero Ohm resistors as a build option.



Users must ensure that system IO levels do not exceed FPGA I/O bank voltage maximums. Failure to do so may result in severe FPGA damage.

Two of the GPIO lines can be used to feed the system monitor ADC built into the FPGA as a build option. Only four GPIO remain available when using the system monitor option. See section 6.1.1.5 for more information on system monitor.

One of the GPIO lines (GPIO 0) can be used as a trigger source for the FPGA as a build option. The system monitor option cannot be used with the GPIO trigger option.

 The GPIO trigger and GPIO system monitor input are not compatible with one another. Only one or the other may be ordered as a build option.

Auxiliary DC power is also available from the GPIO NANO connector with 3.3V standard and 5.0V as a build option.

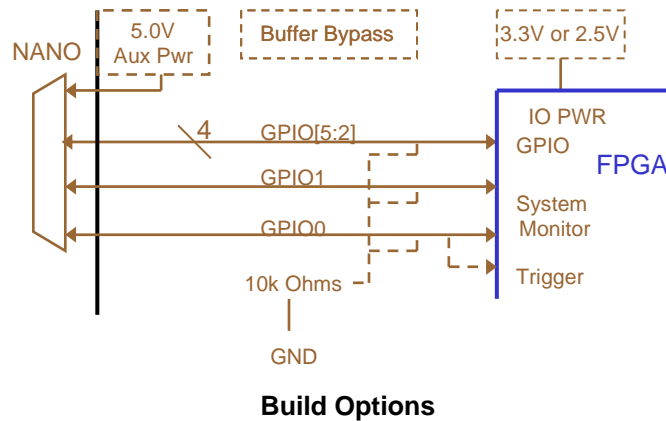
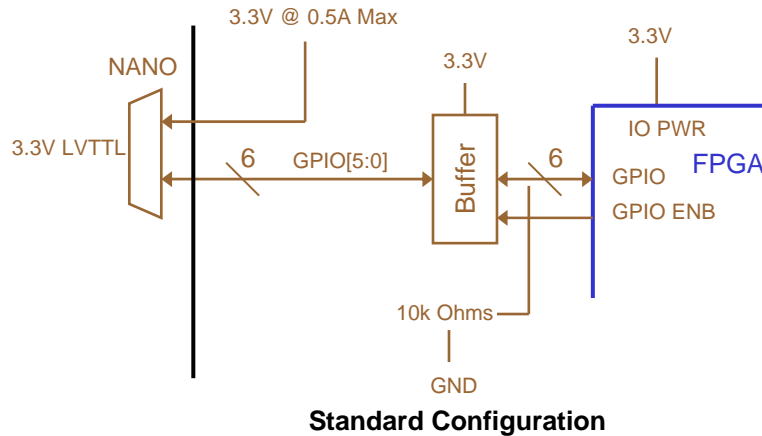


Figure 6-15 GPIO Block Diagram

6.6.2 Coaxial Trigger Interface (Build Option)

The Model 363 contains a coaxial input that can serve as a 50 Ohm terminated LVTTTL external trigger signal as a build option. The input is connected through a single gate 5V tolerant FET buffer directly to the FPGA as shown in Figure 6-16. Trigger input levels are listed in section 3.3. The trigger front panel connection is discussed in section 7.1.

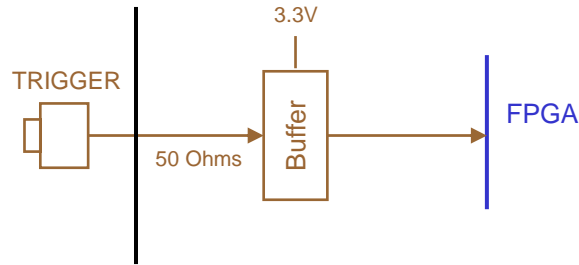



Figure 6-16 Trigger Interface

 Note: the coaxial trigger build option uses the external reference/sample clock connector. An external reference/sample clock cannot be used with the coaxial trigger input build option.

6.6.3 USER IO Interface

There are two user IO ports available for Channel Express as shown in Figure 6-17. The first port consists of FPGA IO routed directly to the legacy PMC P4 connector, the second consists of high-speed serial IO routed directly to the XMC P6 connector. The following paragraphs provide port connectivity details.

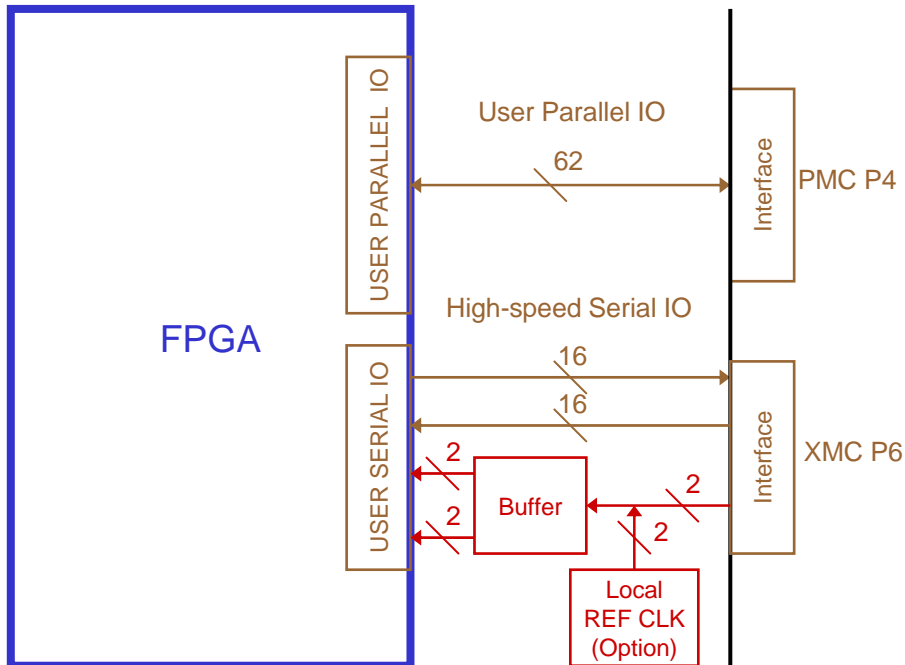


Figure 6-17 User IO Options

6.6.3.1 User Parallel IO (PMC P4)

Channel Express is equipped with a user defined connector that is wired directly to the FPGA user IO interface as shown in Figure 6-18. Users have complete access to the serial IO interface and are free to implement and serial IO standard supported by the FPGA. Some standards are not supported by virtue of the Channel Express hardware configuration. The following paragraphs describe the hardware options available for the USER Parallel IO interface.

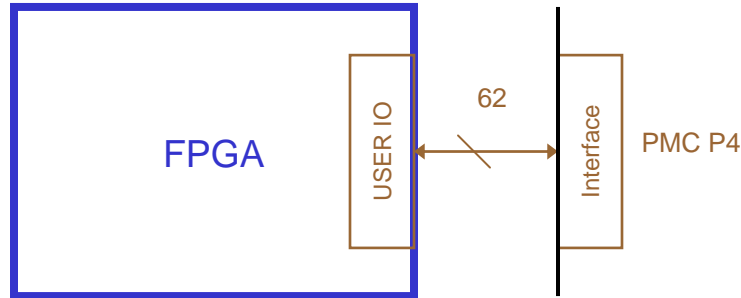


Figure 6-18 USER Parallel IO Interface

The Channel express user IO is wired out as 62 lines arranged as 28 differential pairs plus 6 single ended lines as shown in Figure 6-19. The lines in the differential pairs may also be configured as individual single ended connections. The driver voltage of the user defined I/O bank can be tied to either 2.5 V (default) or 3.3 V as a build option. Two of the lines (User61/62) are also ac-coupled and back terminated to 50 Ohms prior to connection to clock inputs as shown in Figure 6-20. Users should account for this 50 Ohm load if User lines 61 and 62 are not used as clock inputs. The termination can be removed as a build option.

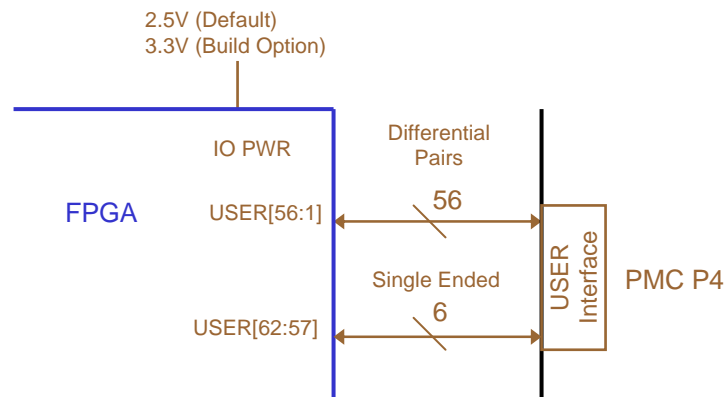


Figure 6-19 USER IO Connections

There are no terminations external to the FPGA; the only mechanism for termination is the DIFF_TERM option in the FPGA IOB. Lines are routed at 50 Ohms nominal impedance and length matched to within 1 inch. See the FPGA data sheet for IO level and switching characteristics. FPGA part number information can be found in Table 6-4. See section 7.3 for connectivity details.

! USER IO is hardwired directly to the FPGA. Users must ensure that system IO levels do not exceed FPGA I/O bank voltage maximums. Failure to do so may result in severe FPGA damage.

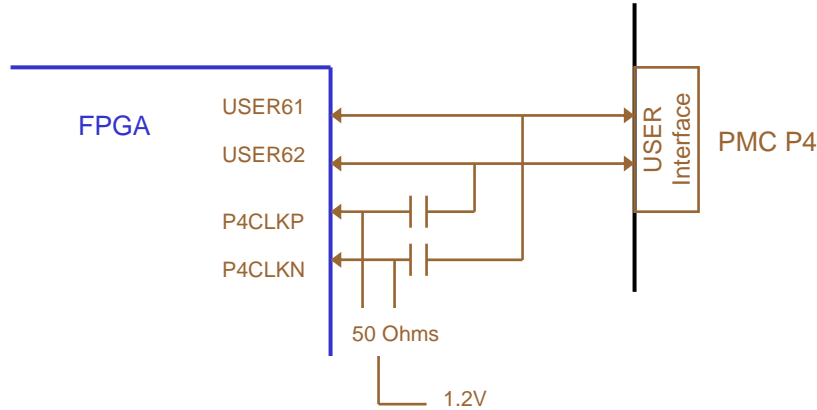


Figure 6-20 Parallel IO Clock Interface

6.6.3.2 High-speed Serial IO (XMC P6)

The Channel Express is equipped with a user defined connector that is wired directly to the FPGA high-speed serial IO interface as shown in Figure 6-21. The user IO interface 16 high-speed serial IO channels arranged as 8 dedicated input and 8 dedicated output differential pairs. The high-speed serial IO lines are connected to MGT interfaces on the FPGA. See section 7.2 for connection details.

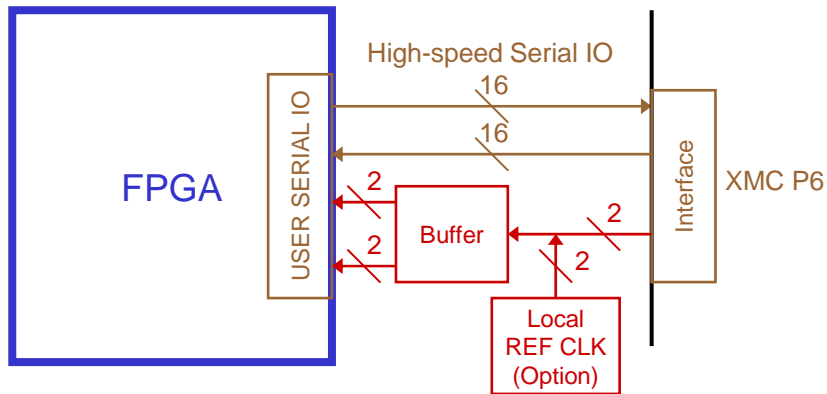


Figure 6-21 USER Serial IO Interface

Channel Express has the facility to operate the serial links from an external reference clock. The clock can be sourced from the XMC P6 connector or from a local source as a build option as shown in Figure 6-22. The buffer is a low voltage CML fanout buffer that serves to split the main clock into two MGT reference clocks, one for each high-speed serial IO bank. Clock level specifications can be found in FPGA vendor data sheet. Clock connectivity information can be found in Table 7-3. Fanout buffer information can be found from the component vendor data sheet referenced in Table 6-4.

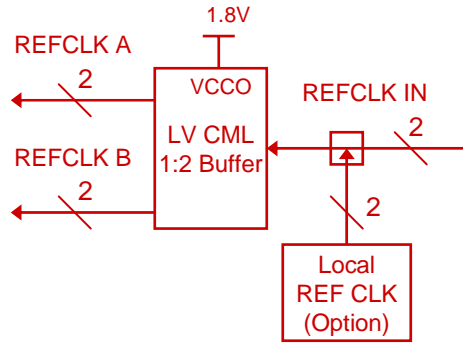



Figure 6-22 USER Serial IO Reference Clock Interface

Users have complete access to the serial IO interface and are free to implement any serial IO standard supported by the FPGA and reference clock structure. The serial links are implemented as transceiver pairs as shown in Figure 6-23. Keep in mind that some standards may not be supported by virtue of pin assignments made on the XMC P6 connector. IO connectivity information can be found in Table 7-3.

 Some IO standards may not be supported by virtue of the pin assignments made on connector P6.

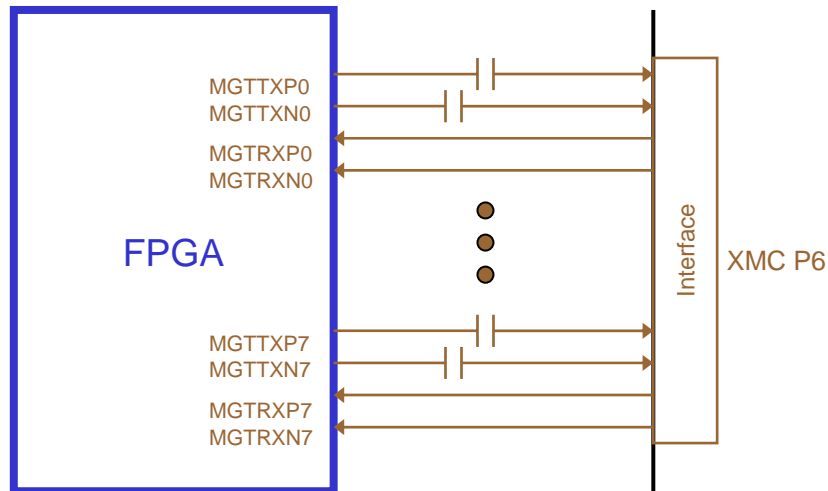



Figure 6-23 USER Serial IO Connections

 USER IO is hardwired directly to the FPGA. Users must ensure that system IO levels do not exceed FPGA I/O bank voltage maximums. Failure to do so may result in severe FPGA damage.

6.6.4 JTAG Interface

The FPGA and Configuration PROM are user programmable devices that can be loaded with application logic directly from the host through a JTAG header. As shown in Figure 6-24, the JTAG chain is composed of the Configuration PROM followed by the FPGA. The configuration PROM may also be loaded through the express bus

interface once an express bus core is loaded into the FPGA. The FPGA itself cannot be directly loaded via the express interface.

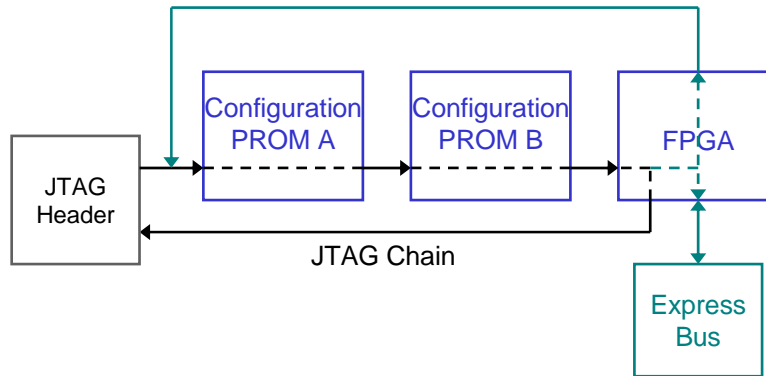


Figure 6-24 JTAG Chain

A JTAG interface header provides access to the Xilinx Configuration PROM and FPGA. The JTAG port can be directly connected to a Xilinx programming cable to configure the devices using the Xilinx iMPACT™ tool or perform debug with Xilinx ChipScope™. See section the *Channel Express FPGA Core Manual* for information on programming the PROM and FPGA via the JTAG port. See section 7.4.1 for JTAG header location and pin descriptions.



The FPGA cannot be directly programmed over the express bus interface since the endpoint core would be written over and lost to the host system during the process.

6.6.5 LED Indicators

Several LED indicators are available on the Model 363 to provide visual configuration confirmation and support integration and test efforts. A detailed list of LED functions and locations can be found in section 7.4.2 of this document.

6.7 Key Components

The key hardware components for the Model 363 assembly are listed in Table 6-4. This information is supplied to assist in the development of custom application logic for the FPGA.

Table 6-4 Key Hardware Components

Component	Part Number	Vendor	Comments
Receiver ADC	ADS5474	TI	14-bit, 400 MSPS, A/D Converter
Offset DAC	LTC1661	Linear Technology	Dual 10-bit Micropower DAC
Virtex-5 FPGA	XC5VLX50T XC5VLX85T XC5VLX110T XC5VSX50T XC5VSX95T	Xilinx	Virtex-5 FPGA w/serial ports LX: High-performance logic SX: Ultra-high-performance DSP
Config PROM	XCF08P XCF32P	Xilinx	Configuration PROMs for the FPGA, the XCF08P is depopulated for smaller gate count parts. See Xilinx data sheet for more information.
Serial EEPROM	AT24C02BN-SH-B	ATMEL	2kb serial EEPROM used for FRU identification storage.
SRAM (Optional)	K7R641882M-FC25	Samsung	QDR II SRAM, 250 MHz
SDRAM (Optional)	MT46H32M32LFCM-6	Micron	1Gb Mobile DDR SDRAM, 6ns, 8MX32b
Single FET Buffer	74CB3T1G125	TI	Single FET bus switch
Octal FET Bus Switch (GPIO Buffer)	74CB3T3245	TI	Octal FET bus switch
LV CML 1:2 Buffer	SY54011RMG	Micrel	Low Voltage 1.2/1.8V CML 1:2 Fanout Buffer, 3.2GHz
Local REF Clock (Optional)	530KB100M000DG	Silicon Labs	OSC CLCC-6 100 MHz 1.8V CML Crystal Oscillator
Low Noise Clock Distribution	AD9512	Analog Devices	1.2 GHz Clock Distribution IC.
Frequency Synth	ASY-817-033	Red Rapids	400 MHz (default) fixed frequency synthesizer.
TCXO	VTC4-A01D-10M000	Vectron	Oscillator, 10 MHz, ± 1.0 ppm
GPIO Connector	83614-9012	Molex	25-circuit right-angle Micro-D connector
GPIO Mating Connector	83424-9021	Molex	25-circuit Micro-D mating connector with 72" pig tail (28 AWG)

7.0 External Interfaces

7.1 Front Panel Interface

There are four external connectors located along the face of the Model 363 module as shown in Figure 7-1. The three coaxial SMA connectors are 50 Ohm terminated analog inputs. Two of the connectors are assigned to the receiver A/B channel signal inputs and the third serves as an external reference/sample clock input (default) or trigger input (build option). A 15-pin high density connector is also provided for general purpose I/O (GPIO) providing 8 digital signals and one DC power pin.

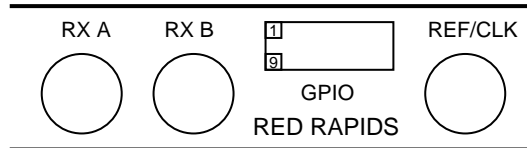


Figure 7-1 Model 363 Front Panel Connectors

Table 7-1 Front Panel Connectors

Des	Label	Connector	Description
J1	RX A	SMA	Receiver Channel A
J2	RX B	SMA	Receiver Channel B
P5	GPIO	High Density 15pin	General Purpose IO
J3	REF/CLK/TRIG	SMA	10 MHz reference/Sample Clock/Trigger

The REF/CLK SMA connector can be configured as an external trigger input as a build option. The trigger input in this case is terminated into 50 Ohms and routed through a 5V tolerant buffer.

GPIO is supplied through an Omnetics Dual Row Nano 15-position connector (PN A28100-015). The pinout for the connector is shown in Table 7-2. The FPGA and buffer output drive source voltage for all designated I/O pins is set to 3.3 V. The GPIO pins use 3.3V LVTTTL protocol, voltage levels are listed in section 3.6. The 3.3V power pin can supply up to 500 mA of current. The same pin can supply 5.0V as a build option.

The mating connector assembly is available from Red Rapids or directly from Omnetics (PN A29000-115). Red Rapids supplies one mating connector cable assembly with each unit. The cable assembly consists of a single mating connector and an 18 inch minimum pigtail. Connector details are shown in Figure 7-3 and Figure 7-3.

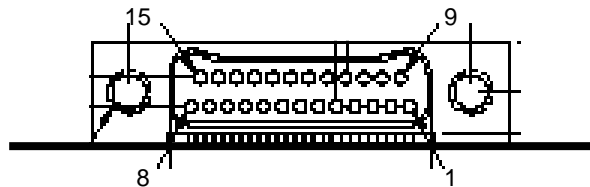


Figure 7-2 General Purpose I/O Connector Detail

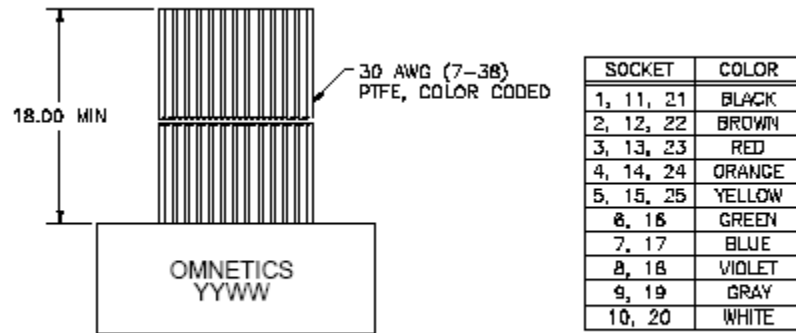


Figure 7-3 General Purpose I/O Mating Cable Connector

Table 7-2 General Purpose I/O Connector Pinout

Pin	Signal Type	Signal Name
1	GND	N/A
2	GND	N/A
3	GND	N/A
4	GND	N/A
5	GND	N/A
6	GND	N/A
7	Power	3.3V (5.0V)
8	I/O/TRIG/SYSMON_P	GPIO0 (Trig)
9	I/O	GPIO7
10	I/O	GPIO6
11	I/O	GPIO5
12	I/O	GPIO4
13	I/O	GPIO3
14	I/O	GPIO2
15	I/O/SYSMON_N	GPIO1

7.2 Host Interface

The host interface for Channel express card is the PCI express bus. The location and pin assignments for the express bus host connector (P5) are dictated by the XMC PCI Express specification. FPGA pin assignments can be found in the FPGA Development Kit UCF supplied with the unit. Pin connections unique to the express card are described in section 6.1.2.

7.3 User IO

Channel Express features two user IO interfaces. The user parallel IO interface consists of 62 lines routed between the FPGA and the PMC P4 connector. The user serial IO interface consists of 16 high-speed differential pairs plus clock routed between the FPGA and the XMC P6 connector. The following sections provide connector pin information.

7.3.1 Parallel User IO (PMC P4)

The PMC P4 connector pin assignments are listed in Table 7-3. FPGA pin assignments can be found in the UCF file provided with the FPGA development kit download. A description of the user parallel IO interface can be found in section 6.6.3.1.

Table 7-3 PMC P4 User Defined Connector Pinout

Name	P4 Pin	P4 Pin	Name
USER1(N1)	1	2	USER2(N2)
USER3(P1)	3	4	USER4(P2)
USER5(N3)	5	6	USER6(N4)
USER7(P3)	7	8	USER8(P4)
USER9(N5)	9	10	USER10(N6)
USER11(P5)	11	12	USER12(P6)
USER13(N7)	13	14	USER14(N8)
USER15(P7)	15	16	USER16(P8)
USER17(N9)	17	18	USER18(N10)
USER19(P9)	19	20	USER20(P10)
USER21(N11)	21	22	USER22(N12)
USER23(P11)	23	24	USER24(P12)
USER25(N13)	25	26	USER26(N14)
USER27(P13)	27	28	USER28(P14)
USER29(N15)	29	30	USER30(N16)
USER31(P15)	31	32	USER32(P16)
USER33(N17)	33	34	USER34(N18)
USER35(P17)	35	36	USER36(P18)
USER37(N19)	37	38	USER38(N20)
USER39(P19)	39	40	USER40(P20)
USER41(N21)	41	42	USER42(N22)
USER43(P21)	43	44	USER44(P22)
USER45(N23)	45	46	USER46(N24)
USER47(P23)	47	48	USER48(P24)
USER49(N25)	49	50	USER50(N26)
USER51(P25)	51	52	USER52(P26)
USER53(N27)	53	54	USER54(N28)
USER55(P27)	55	56	USER56(P28)
USER57	57	58	USER58
USER59	59	60	USER60
USER61 ⁽¹⁾	61	62	USER62 ⁽¹⁾
NC	63	64	NC

Notes:

- (1) Pins highlighted in yellow are ac-coupled and back terminated into 50 Ohms, see Figure 6-20 for more information.

7.3.2 Serial User IO (XMC P6)

The XMC P6 connector pin assignments are listed in Table 7-4. FPGA pin assignments can be found in the UCF file provided with the FPGA development kit download. A description of the user serial IO interface can be found in section 6.6.3.2.

Table 7-4 User Serial IO Pin Connections

	A	B	C	D	E	F
01	TXSIOp0	TXSIOn0	NC	TXSIOp1	TXSIOn1	NC
02	GND	GND	NC	GND	GND	NC
03	TXSIOp2	TXSIOn2	NC	TXSIOp3	TXSIOn3	NC
04	GND	GND	NC	GND	GND	NC
05	TXSIOp4	TXSIOn4	NC	TXSIOp5	TXSIOn5	NC
06	GND	GND	NC	GND	GND	NC
07	TXSIOp6	TXSIOn6	NC	TXSIOp7	TXSIOn7	NC
08	GND	GND	NC	GND	GND	NC
09	NC	NC	NC	NC	NC	NC
10	GND	GND	NC	GND	GND	NC
11	RXSIOp0	RXSIOn0	NC	RXSIOp1	RXSIOn1	NC
12	GND	GND	NC	GND	GND	NC
13	RXSIOp2	RXSIOn2	NC	RXSIOp3	RXSIOn3	NC
14	GND	GND	NC	GND	GND	NC
15	RXSIOp4	RXSIOn4	NC	RXSIOp5	RXSIOn5	NC
16	GND	GND	NC	GND	GND	NC
17	RXSIOp6	RXSIOn6	NC	RXSIOp7	RXSIOn7	NC
18	GND	GND	NC	GND	GND	NC
19	SIREFCLKP	SIREFCLKN	NC	NC	NC	NC

7.4 Board Interface

7.4.1 JTAG Interface

Figure 7-4 illustrates the location of the JTAG connector on the Model 363 close to U37. The header consists of six recessed pin receptacles spaced on 0.1 inch centers. The receptacle will accept a 0.022 inch to 0.034 inch diameter pin or a 0.025 inch square pin. The flying leads supplied with the Xilinx programming cable are compatible with the receptacles. All of the pins except TRSTB must be connected for programming.

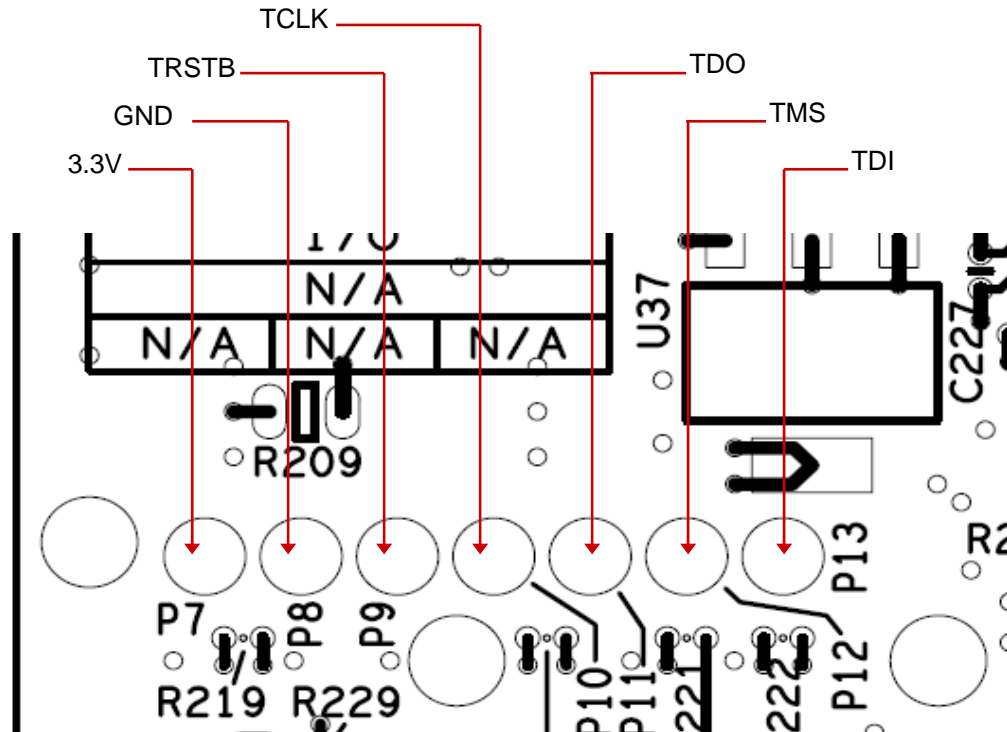


Figure 7-4 JTAG Header Location

Table 7-5 lists the mapping of pin reference designators on the PWB to the corresponding JTAG signal name.

Table 7-5 JTAG Header Signal Mapping

Reference Designator	Signal Name
P7	3.3V
P8	GND
P9	TRSTB
P10	TCLK
P11	TDO
P12	TMS
P13	TDI

7.4.2 PMC LED Indicators

There are several LED indicators that report various hardware status functions as listed in Table 7-6. Two of the LEDs (D6 & D7) are tied to a bit in the *LED Control* register which can be toggled from application software.

Table 7-6 LED Operating Status Indicators

Reference Designator	Color	Status (Illuminated)
D1	Yellow	User LED "A" active.
D2	Green	User LED "B" active.
D3	Red	Internal synthesizer fault (not locked).
D4	Yellow	External 10 MHz reference clock active.
D5	Green	Internal 10 MHz reference clock active.
D6	Yellow	External sample clock active.
D7	Green	Internal sample clock active.

The diode locations are shown in Figure 7-5.

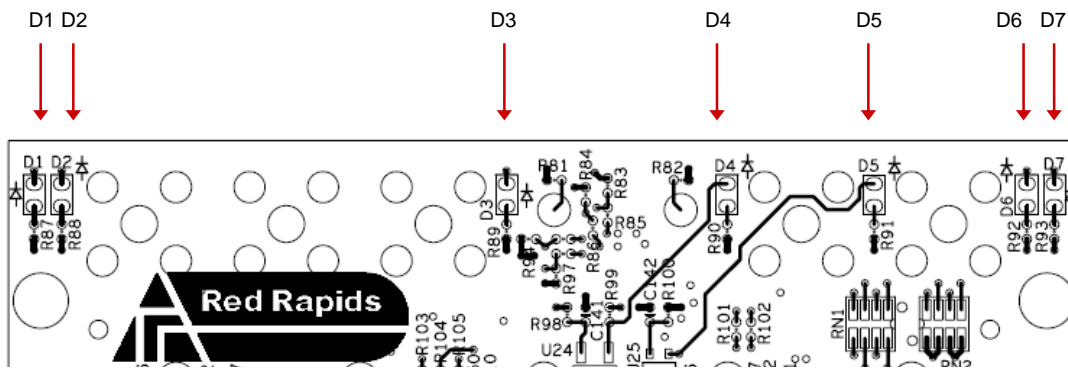


Figure 7-5 Diode Location

8.0 Build Options

Red Rapids typically stocks the board configurations listed in Table 8-1 and standard on-board synthesizer frequencies shown in Table 8-2.

Table 8-1 Model 363 Standard Board Configurations

FPGA	SRAM	USER IO Voltage	GPIO Buffer	J3 Coax Connector	GPIO DC Power	GPIO Pin 0 Trigger	RX Coupling
XC4VSX55-11	No SRAM	2.5V	Installed	REF/CLK	3.3V	No (GPIO0)	AC
XC4VSX55-11	32 MB	2.5V	Installed	REF/CLK	3.3V	No (GPIO0)	AC

Table 8-2 Model 363 Standard Synthesizer Frequencies

Standard Synthesizer Frequencies (MHz)
213.3, 400

The Model 363 can be ordered with different build options as listed in Table 8-3. Build options may be ordered independent of one another.

Table 8-3 Model 363 Build Options

Item	Options
FPGA	XC4VLX40 XC4VLX100 XC4VLX160 XC4VSX55*
FPGA Speed Grade	-11* -12
SRAM	No SRAM* 32 MB SRAM*
Receiver Coupling	AC* DC
User IO Voltage	2.5V* 3.3V
GPIO Buffer	Installed* Bypassed
J3 Coax Connector	REF/CLK* Trigger
GPIO DC Power	3.3V* 5.0Vr
GPIO0	GPIO0* Sys Mon P Trigger
GPIO0	GPIO1* Sys Mon N
Custom Synthesizer	50 - 400 MHz

Note: * items are default/standard

Non-standard configurations are built to order and subject to being non-cancelable/non-returnable. Delivery lead times are subject to component availability at time of order.

9.0 Technical Support

Please feel free to contact us if you have a technical question about or problem with our product. We understand that our customers have tight deadlines and time is of the essence in development and production cycles. We will make every effort to resolve problems as quickly as possible.

Web: www.redrapids.com

Email: support@redrapids.com

Phone: 972-671-9570

Fax: 972-671-9572

Please include the following information with your correspondence:

Contact Information

Product Model

Host Card or System (PC, PCI Carrier, Single Board Computer)

Operating System

Problem Description