

Model 361 Channel Express RX2 16/160 Hardware Reference Manual



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1.0 Introduction

1.1 Contents and Structure

This manual describes the Model 361 Channel Express hardware and in conjunction with the items listed in the supporting documents of section 1.2 provides a complete description of the capabilities and operation of this product. The focus of this manual is the electrical function of the hardware including control structure, signal flow, clock distribution, external interfaces and key components. Other Channel Express manuals focus on software and the internals of the FPGA.

The manual is divided into nine sections as follows:

Section	Description
Section 1	Introductory information about the manual.
Section 2	Product overview.
Section 3	Hardware specifications.
Section 4	Absolute maximum conditions without damage.
Section 5	Hardware performance characteristics.
Section 6	Detailed hardware description.
Section 7	External interface descriptions and connector pinouts.
Section 8	Hardware build options
Section 9	Technical support

The latest product documentation and software is available for download from the Red Rapids web site (www.redrapids.com) by following the Technical Support link.

1.2 Supporting Documents


Author	Number	Title
Red Rapids	REF-360-001	Channel Express Installation Guide
Red Rapids	REF-360-002	Channel Express Software Reference Manual
Red Rapids	REF-360-003	Channel Express FPGA Core Manual
ANSI/VITA	42.0-2005	XMC Switched Mezzanine Card Auxiliary Standard
ANSI/VITA	42.3-2006	XMC PCI Express Protocol Layer Standard
PCI SIG	PCI Express Base Rev 1.1	PCI-SIG, PCI Express Base Specification Revision 1.1

1.3 Conventions

This manual uses the following conventions:

- Hexadecimal numbers are prefixed by “0x” (e.g. 0x00058C).
- *Italic* font is used for names of registers.
- **Bold** font is used for names of directories, files and OS commands.
- Palatino font is used to designate source code.
- Active low signals are followed by ‘#’, For example, TRST#.

 Text in this format highlights useful or important information.

 Text shown in this format is a warning. It describes a situation that could potentially damage your equipment. Please read each warning carefully.

The following are some of the acronyms used in this manual.

- | | |
|---------------------|--|
| • ADC | Analog to Digital Converter |
| • API | Application Program Interface |
| • CMC | Common Mezzanine Card |
| • CPCI | CompactPCI |
| • DAC | Digital to Analog Converter |
| • DCM | Digital Clock Manager |
| • DMA | Direct Memory Access |
| • FRU | Field Replaceable Unit |
| • GPIO | General Purpose Input/Output |
| • IDELAY | Virtex Input Delay Element |
| • IDELAYCTRL | Virtex Input Delay Control Element |
| • IOB | Virtex Input/Output Block |
| • MSPS | Mega Samples per Second |
| • PCI | Peripheral Component Interconnect |
| • PMC | PCI Mezzanine Card |
| • QDR | Quad Data Rate |
| • SFDR | Spur Free Dynamic Range |
| • SINAD | Signal-to-Noise and Distortion |
| • SNR | Signal-to-Noise Ratio |
| • TCXO | Temperature Compensated Crystal Oscillator |
| • UCF | Virtex User Constraints File |

1.4 Manual Compatibility

The applicable hardware part numbers are defined as follows:

- Model 361-XXX⁽¹⁾ *Channel Express 16/160*

⁽¹⁾ XXX is a three digit number that indicates the hardware variant.

1.5 Revision History

Version	Date	Description
R00	6/10/2010	Initial release.

2.0 Overview

The Channel Express product family provides the ideal platform to rapidly field application specific I/O functions minus the expense of custom hardware development. The architecture features a high performance front-end tightly coupled to a Xilinx Virtex-5 FPGA. The FPGA communicates directly with the host processor through the PCI Express interface. Simple interfaces to the ADC, I/O, SRAM and SDRAM are easily integrated with user application logic.

The Channel Express product family offers several different front-end hardware options. The Model 361, illustrated in Figure 2-1, provides a dual channel digitizer based on the Linear Technologies LTC2209 (16-bit/160Msps) A/D converter (ADC).

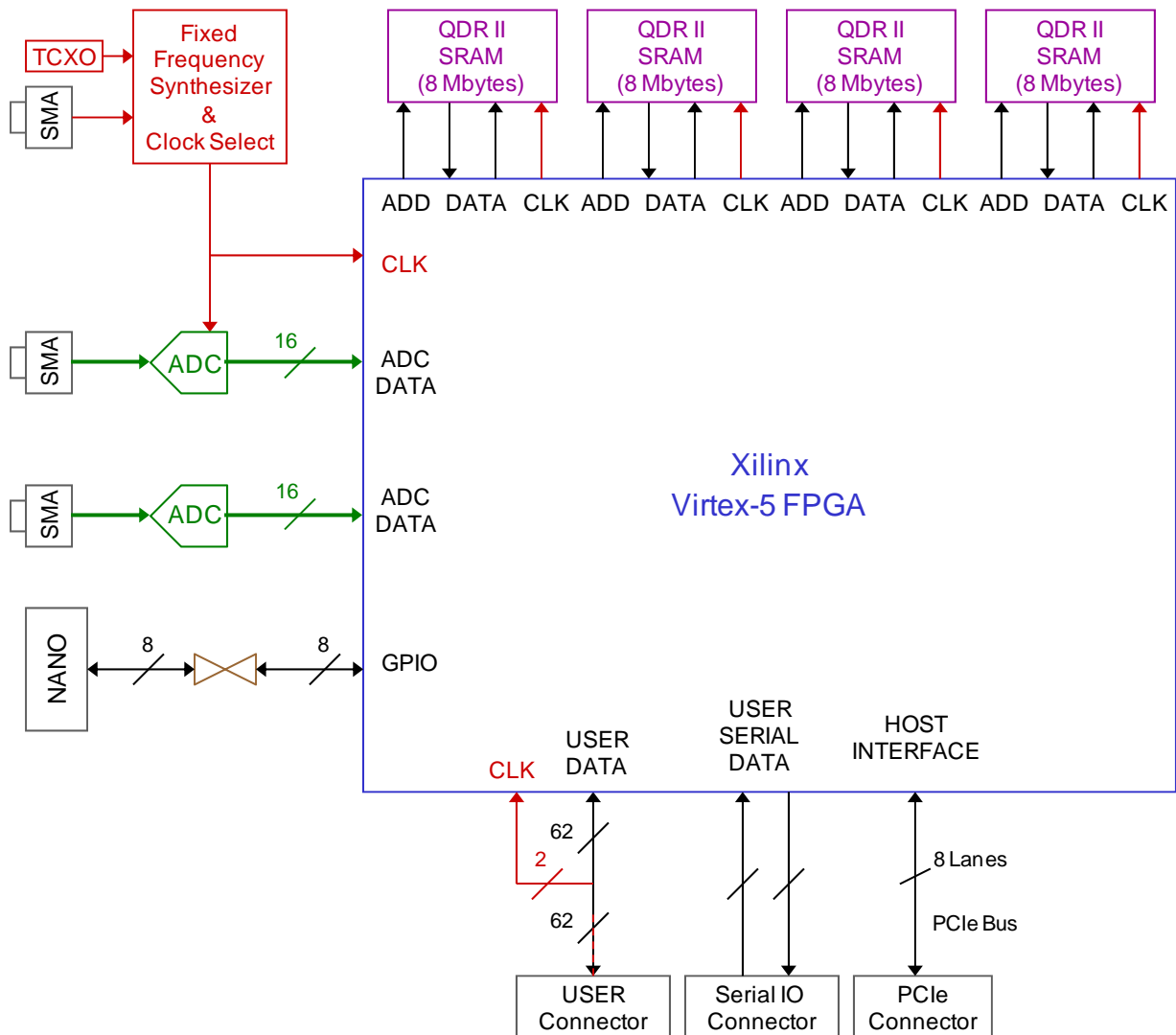


Figure 2-1 Model 361 Block Diagram

The receiver sample clock is supplied by an on-board frequency synthesizer or an external source. The frequency synthesizer can be phase locked to the local 10 MHz temperature compensated crystal oscillator (TCXO) or an external reference can be used to achieve system-wide phase coherence.

The FPGA can be selected from the Virtex-5 high performance logic (LX) or signal processing (SX) platforms. A variety of size and speed grade options are offered to further optimize the price/performance ratio over a wide range of applications.

The FPGA can be connected to four optional 16-bit QDR SRAMs for high speed local data storage. The QDR SRAM provides separate read and write ports to maximize data transfer into and out of memory. This memory can also be used as a high-speed snapshot recorder to store segments of data without interruption from PCIe bus traffic.

A GPIO connector offers six general purpose digital I/O ports, a 50 ohm terminated trigger input, and access to the System Monitor ADC internal to the FPGA.

Users also have access to two general IO ports connected directly from the FPGA to two external connectors. One IO port provides parallel access across 62 lines while the other provides high-speed serial access to the FPGA MGT interface over eight bidirectional differential transceivers.

The host Interface implements the industry standard PCI express bus for high-speed communication between the host and card using up to 8 express lanes. The PCI Express standard is supported by a wide variety of host systems for data communication applications.

A DMA FPGA core is provided to manage data transfers between Channel Express and host memory. The DMA engine allows the receiver to automatically initiate a PCI burst transaction when a predetermined number of samples are available. An interrupt is generated by Channel Express when the specified number of data blocks have been written.

There are also more sophisticated DMA features built into the core. DMA chaining and scatter-gather techniques are supported by both the hardware and software to optimize data transfer efficiency. Refer to the product *Channel Express FPGA Core Manual* for further details.

The Virtex-5 FPGA is supported by a robust set of development tools from Xilinx. Creation of user configuration code follows the standard design flow using a pin assignment file supplied with Channel Express. VHDL source code for the ADC, and SRAM are also provided. The PROM and FPGA can be loaded through a JTAG connector using Xilinx iMPACT software.



The Channel Express product is intended for users with significant experience in FPGA design. As an alternative Red Rapids offers a line of fixed function products to meet standard data acquisition needs which require no FPGA design experience.

3.0 Hardware Specifications


All specifications estimated unless otherwise noted.

3.1 Board Specification Summary

Specification	Value
Physical	
XMC	VITA 42.0
Weight	3.8 ounces
Electrical	
Supply Voltages	3.3V, +12V, VPWR (+5V or +12V)
Bus Protocol	VITA 42.3 (PCI Express 1.0, Up to 8 Lanes)
Vendor ID (Hex)	0x17D2
Device ID (Hex)	0x00CA
Power (max) ⁽¹⁾	(see notes below)
Analog (AC-Coupled)	6.8 W (Not including digital)
Analog (DC-Coupled)	7.5 W (Not including digital)
Digital (No SRAM)	0.6 W (Not including FPGA)
Digital (32 MB SRAM)	10 W (Not including FPGA)
FPGA Core Current Limit	FPGA core current (1.0V) is limited to 12A
Environmental⁽²⁾	
Airflow (minimum)	250 LFM
Operating (Inlet Air)	
Temperature	0°C to 35°C Ambient
Humidity	90% maximum (non-condensing)
Altitude	15,000 Feet
Non-Operating	
Temperature	-20°C to 65°C Ambient
Humidity	95% maximum (non-condensing)
Altitude	40,000 Feet

⁽¹⁾The power dissipation of the FPGA is not included in section 3.1 since it depends on the specific application bitstream that is loaded. A power calculator spreadsheet is offered by Red Rapids to assist in the total power calculation for a specific application.

⁽²⁾The hardware has not been tested to the environmental specification listed in section 3.1.

	The maximum amount of FPGA core current (1.0V) supported by Channel Express is 12A.
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3.2 Receiver Specifications

3.2.1 Receiver Input Levels

Parameter	Min	Typ	Max	Unit
Input Impedance		50		Ohms
ADC Offset Error ⁽¹⁾	-8.5	+/-2	+8.5	mV
DC Coupling Offset Error ⁽¹⁾	-50		+50	mV
Full Scale Input (0 dBFS, 50 ohms)				
High Voltage Range(default)				
Input Voltage		2.4		Vpp
Input Power		+11.5		dBm
Low Voltage Range				
Input Voltage		1.6		Vpp
Input Power		+8.0		dBm

Notes: ⁽¹⁾ ADC offset dominates when AC coupled; DC coupling circuit offset dominates when DC coupled.

3.3 External Reference/Clock/Trigger Input Levels

Parameter	Min	Typ	Max	Unit
External Reference (REF)				
Input Impedance		50		Ohms
Input Voltage (50 Ohms)	1.5		3.5	Vpp
Input Power (50 Ohms)	+7		+14.8	dBm
Frequency	10		10	MHz
External Clock Input (CLK IN)				
Input Impedance		50		Ohms
Input Voltage (50 Ohms)	0.8	2.8	2.8	Vpp
Input Power ⁽¹⁾ (50 Ohms)	+2	+13	+13	dBm
Frequency	236 ⁽²⁾		400	MHz
Trigger Input (TRIG)				
Input Impedance		50		Ohms
VIL	-0.5		0.8	V
VIH	2.4		5.5	V

Notes: ⁽¹⁾ See external clock discussion on square vs. sine input.

⁽²⁾ Minimum DCM setting for Diagnostic program, User may change the DCM setting to values as low as 50MHz.

3.4 Internal Clock Performance

Parameter	Min	Typ	Max	Unit
Internal Sample Clock				
Frequency (default)		160		MHz
Reference Spurs			75	dBc
Phase Noise				
1 kHz offset		-90		dBc/Hz
10 kHz offset		-100		dBc/Hz
100 kHz offset		-120		dBc/Hz
Internal Reference				
Frequency (default)		10		MHz
Stability	-1.0		+1.0	ppm
Phase Noise				
1 kHz offset		-125		dBc/Hz
10 kHz offset		-145		dBc/Hz
100 kHz offset		-148		dBc/Hz

3.5 USER IO Voltage Levels

The table below provides voltage levels for LVTTTL modes of operation. Due to the wide variety of IO standards supported by direct connection to the FPGA, users should refer to the FPGA data sheet for voltage level information for non LVTTTL modes.

Parameter	Min	Typ	Max	Unit
3.3V LVTTTL				
VIH	2.0		3.45	V
VIL	-0.2		0.8	V
VOH	2.4			V
VOL			0.4	V
IIN		+/-5		uA
IOH at VOH ⁽¹⁾	-24			mA
IOL at VOL ⁽¹⁾			24	mA

⁽¹⁾Current determined by FPGA drive strength setting.

3.6 GPIO Voltage Levels

The table below provides voltage levels for LVTTL modes of operation. Due to the wide variety of IO standards supported by direct connection to the FPGA, users should refer to the FPGA data sheet for voltage level information for non LVTTL modes.

Parameter	Min	Typ	Max	Unit
3.3VLVTTL				
Input Impedance		10k		Ohms
VIH (with buffer)	2.0		5.5	V
VIH (without buffer)	2.0		3.45	V
VIL	-0.2		0.8	V
VOH	2.4			V
VOL			0.4	V
IOH at VOH ⁽¹⁾	-24			mA
IOL at VOL ⁽¹⁾			24	mA
3.3V Aux Power Option				
Voltage Output	3.1	3.3	3.5	V
Current			0.5	A

⁽¹⁾Current determined by FPGA drive strength setting.

4.0 Absolute Maximum Specifications

Stresses above those listed in Table 4-1 may cause damage to the unit. The operation of the unit at these or any other conditions outside of those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may degrade unit reliability.

Table 4-1 Absolute Maximum Specifications

Parameter	Min	Typ	Max	Unit
Environmental (Inlet Air)				
Operating Temperature	-30		50	C
Non-Operating Temperature	-30		85	C
Airflow	250			LFM
Receiver Inputs (50 Ohms)				
AC-Coupled				
DC Input Voltage	-10		10	V
AC Voltage Swing			5	Vpp
AC Input Power			+18	dBm
DC-Coupled				
DC Input Voltage	-3		3	V
AC Voltage Swing			5	Vpp
AC Input Power			+18	dBm
Reference Clock Input (50 Ohms)				
DC Level	-10		10	V
AC Swing			4.5	Vpp
AC Power			+17.5	dBm
Sample Clock Input (50 Ohms)				
DC Level	-10		10	V
AC Swing			4	Vpp
AC Power			+16	dBm
GPIO				
Buffered inputs	-0.5		5.0	V
Un-buffered inputs (Bypass)				
2.5V Power Rail	-0.5		2.8	V
3.3V Power Rail	-0.5		3.6	V
USER IO				
2.5 V IO Power Rail	-0.5		2.8	V
3.3 V IO Power Rail	-0.5		3.6	V



Exposure to absolute maximum conditions for extended periods may degrade unit reliability.

5.0 Hardware Description

A high-level block diagram of the M361 Channel Express card is shown in Figure 5-1. The hardware description is divided into seven sections consisting of FPGA, receiver, sample clock distribution, SRAM, SDRAM, IO and key components. The following paragraphs provide a detailed description of each section.

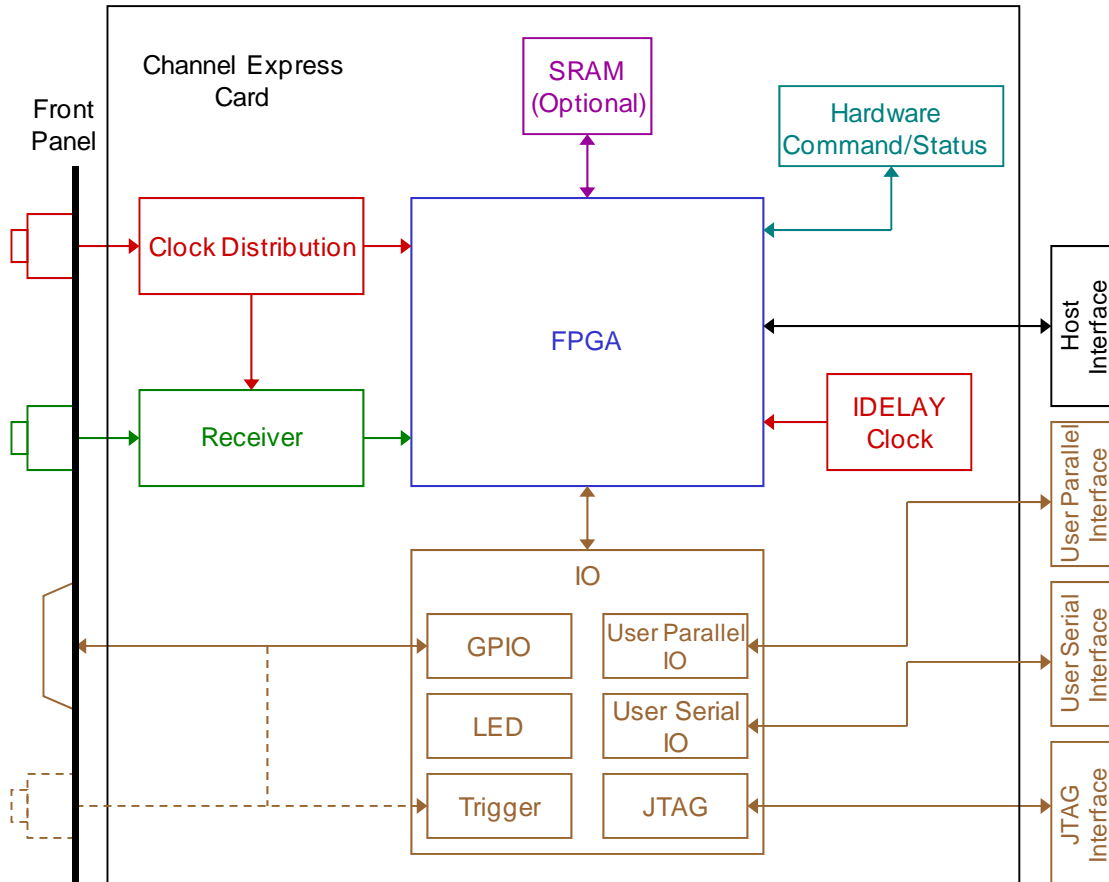


Figure 5-1 Model 361 Hardware Block Diagram

5.1 FPGA

A high-level block diagram of the FPGA with internal cores and interfaces is shown in Figure 5-2. Red Rapids provides FPGA cores to the ADC, SRAM, and Host Interface to ease integration of FPGA application code with the Channel Express hardware. The IO interfaces are governed by the FPGA User Constraints File (UCF) supplied along with the cores. An external 200 MHz oscillator is available as a source for IDELAY configuration within the FPGA.

Refer to the *Channel Express Core Reference Manual* for further details.

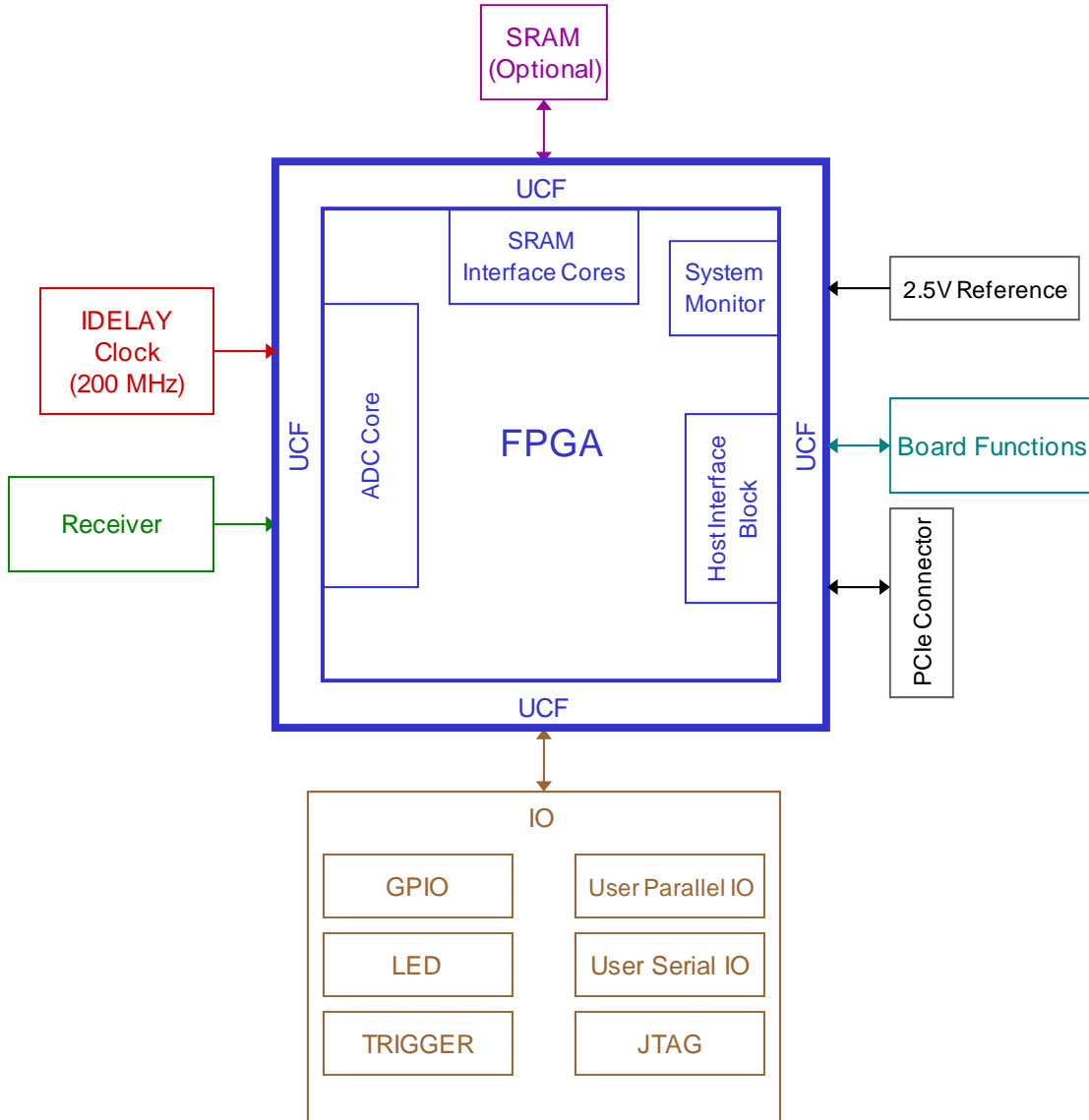


Figure 5-2 FPGA Cores and Interfaces

5.1.1 System Monitor

Every member of the Virtex-5 FPGA family contains a single System Monitor, located in the center of the die. The System Monitor function is built around a 10-bit, 200-kcps ADC. The ADC is used to measure FPGA physical operating parameters like on-chip power supply voltages and die temperatures. External analog inputs allow the ADC to monitor the physical environment of the board or enclosure. System Monitor is fully functional on power up.

Red Rapids supports the built-in System Monitor feature of the Virtex-5 through the addition of an external precision 2.5V reference. The system monitor dedicated differential analog input has also been brought out on a pair of general purpose IO pins as shown in Figure 5-3. For more information on GPIO see section 5.5.1. Specific part information on the 2.5V reference can be found in the vendor sheet. Voltage reference part number can be found in section 5.6. Connector pin out information can be found in section 6.1.

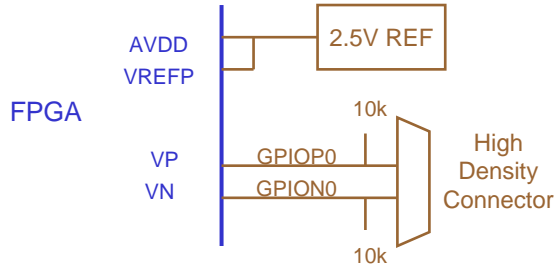


Figure 5-3 System Monitor Support

Please note that system monitor is a Xilinx primitive. Please refer system monitor support questions to Xilinx.

5.1.2 Host Interface Connector

The Host interface connector is defined by the ANSI/VITA XMC PCIe specification in terms of connector location and pin assignment. FPGA connections are listed in the UCF file found in the FPGA Development Kit download for the applicable Channel Express card. A diagram showing board connectivity for ancillary signals is displayed in Figure 5-4. The diagram shows connections made to the on-board serial PROM, JTAG interface and FPGA reset.

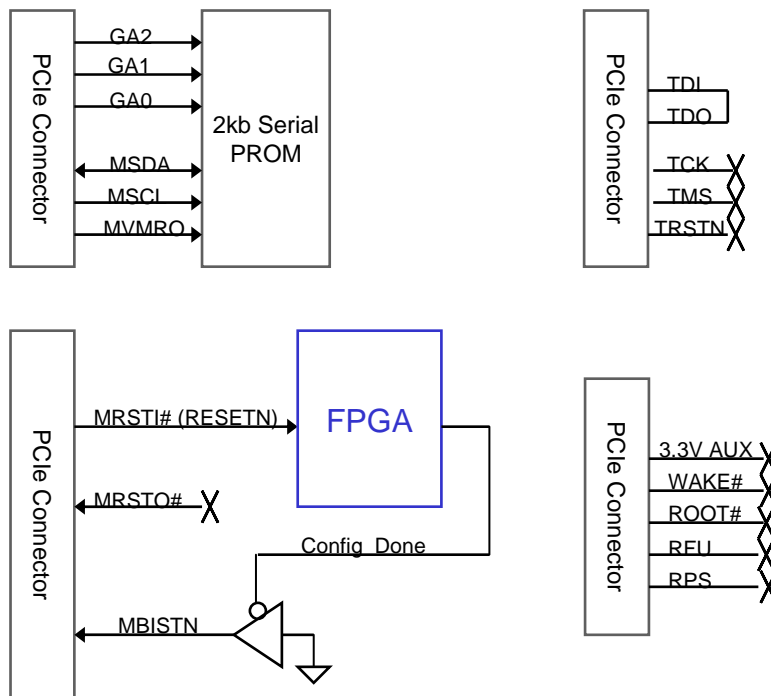


Figure 5-4 Host Interface Connection Detail

5.1.3 FPGA Build Options

The Channel Express Plus family provides for a wide selection of FPGA build options enabling the user to optimize their hardware for a variety of applications. The list of supported FPGA devices can be found in Table 5-1.

Table 5-1 Channel Express FPGA Options


Component	Part Number	Vendor	Comments
Virtex-5 FPGA	XC5VLX50T	Xilinx	Virtex-5 FPGA w/ Serial Links LX: High-performance logic SX: Ultra-high-performance DSP
	XC5VLX85T		
	XC5VLX110T		
	XC5VLX155T		
	XC5VSX50T		
	XC5VSX95T		

5.1.4 FPGA Device Configuration

User configurations are developed using Xilinx standard design flow and tools. Once designs are compiled they can be loaded into the FPGA using one of two methods:

1. The FPGA can be loaded indirectly from a configuration PROM available for non-volatile storage of a bitstream that will load automatically at power-on.
2. The FPGA can be loaded directly through the JTAG connector using the Xilinx IMPACT software.

More information on JTAG programming can be found in section 5.5.4.

 The FPGA cannot be directly programmed over the express bus interface since the endpoint core would be written over and lost to the host system during the process.

5.1.5 FPGA Power Utilization

The high performance capabilities of the Channel Express card can result in significant power consumption requirements and subsequent thermal considerations. This issue is of particular concern in units populated with high gate count FPGAs and large memory configurations. Unfortunately power consumption is a direct function of FPGA gate utilization, memory use and clock speed and thus highly application dependent. The following description is designed to provide the user with guidelines based on our analysis and customer experience to help provide some bounds to the problem.

The first step in the evaluation process is to estimate power consumption using the FPGA power estimation tool (a download from FPGA vendor) and values from section 3.1. Bear in mind that the results from the FPGA power estimation tool vary greatly with design assumptions. Once an initial estimate is made the power consumption requirement should be assessed in terms of the categories outlined in Table 5-2. This process should be repeated as the FPGA design is refined over time.

Table 5-2 Design Risk by Power Category

Power Consumption	Design Risk	Comments
<15 W	Low	Designs in this category have little or no thermal or supply issues as long as cooling air requirements are met.
15 -25 W	Med	Designs in this category should have detailed power estimation performed and system thermal management approach assessed.
>25 W	High	Designs in this category should look to reduce or offload processing and external memory usage. Designs will likely require added thermal management.

5.2 Receiver

A block diagram of the receiver is shown in Figure 5-5. The receiver consists of two independent analog channels labeled A and B. Each channel is accessed through an SMA connector and sampled by an ADC. The ADC sample clock is sourced by the clock distribution section. Each ADC output consists of a 16-bit data word and an overflow bit that connects to the FPGA. See the *Channel Express FPGA Core Reference Manual* for more information on the ADC/FPGA interface.

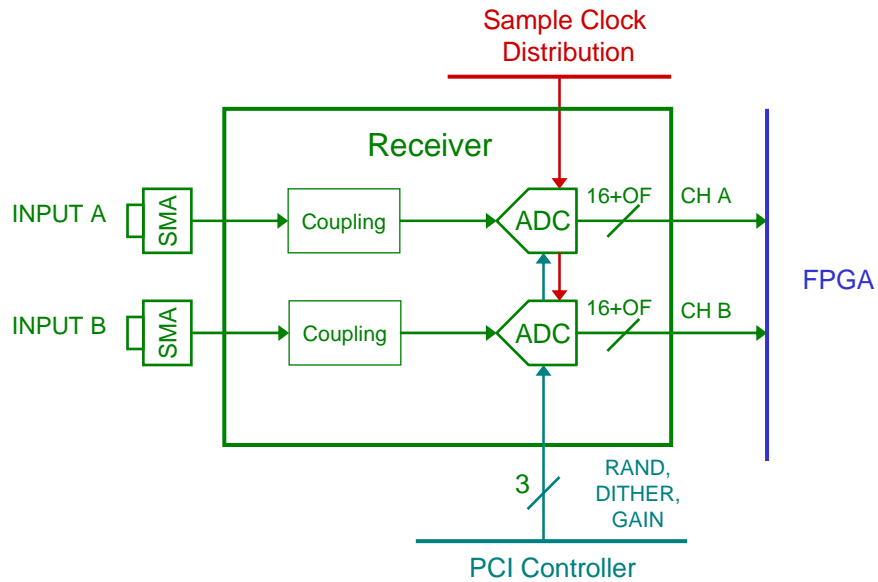


Figure 5-5 Receiver Block Diagram

The Model 361 receiver is available in one of two coupling options, AC or DC. The AC-coupled option provides better dynamic performance at the expense of frequency response below 1 MHz. The DC-coupled option provides coverage below 1 MHz but performance deteriorates as signal frequency content rises above 20 MHz.

Three control signals are available to tailor the performance of the 331 ADC via the FPGA. The three signals are: RAND, DITHER and GAIN. The RAND control enables randomization of the ADC digital data output to reduce interference. The DITHER control enables the randomization of the ADC transfer curve to help reduce spurious at low input signal levels. GAIN control selects between a high or low input voltage range for the ADC. For more information see the data sheet for the receiver ADC listed in the key hardware components list of Table 5-4 and the *Channel Express Software Reference Manual* for detailed information.

The hardware configuration for each Model 361 ADC is summarized in Table 5-3. Receiver input levels are listed in the receiver interface description of section 3.2.1.

Table 5-3 Model 331 ADC Hardware Configuration

Item	Setting	Description
SENSE	VDD	Internal reference selected
SHDN	Ground	ADC shutdown disabled
DITH	FPGA Control	ADC DITH under software control

RAND	FPGA Control	ADC RAND under software control
PGA	FPGA Control	ADC GAIN under software control.
MODE	2/3 VDD	2's complement and clock duty stabilizer selected.
LVDS	VDD	Standard LVDS output selected.

5.3 Sample Clock Distribution

The board sample clock synchronizes the digitization and data movement functions of the Channel Express card. A block diagram of the Model 361 sample clock distribution system is shown in Figure 5-6. The clock can be sourced internally or externally and serves to time data acquisition into the FPGA. The following paragraphs provide more detail on the clock distribution network.

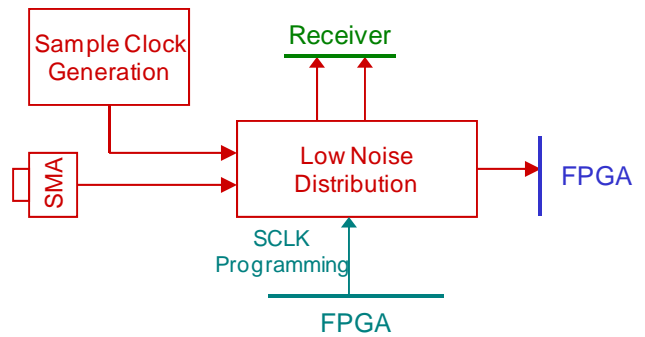


Figure 5-6 Model 361 Clock Distribution

5.3.1 Sample Clock Generator

The Model 361 sample clock may be generated from an on-board fixed frequency synthesizer or a user supplied external clock as shown in Figure 5-7. Power detectors are used to determine the presence of a sample clock or reference and notification is provided to the board control core.

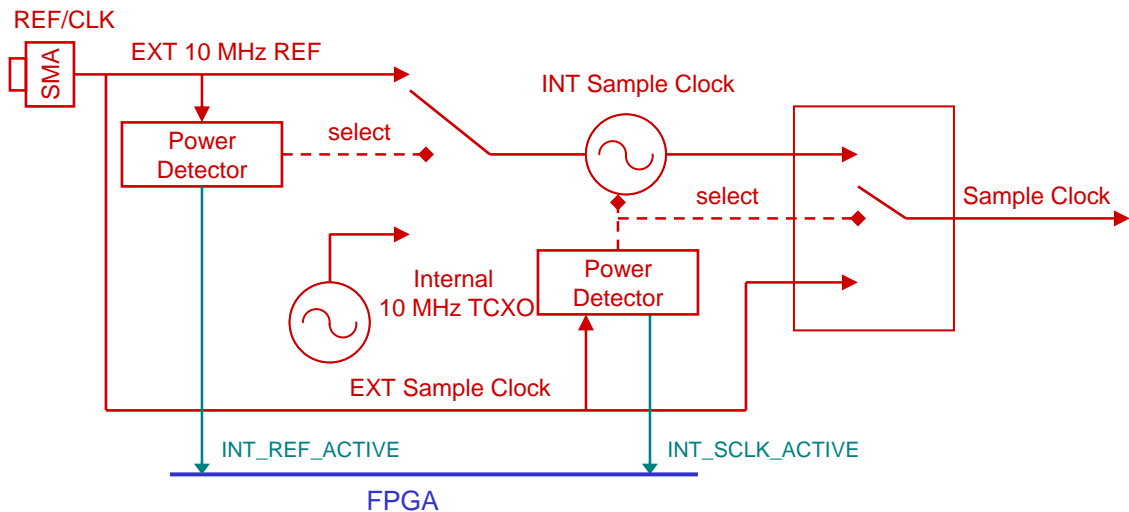


Figure 5-7 Sample Clock Generation



The on-board synthesizer does not operate when an external sample clock is present.

5.3.1.1 External Sample Clock

An external sample clock signal is usually supplied by a high quality source that can provide good frequency stability ($< \pm 2$ ppm) and low phase noise (< 90 dBc/Hz @ 10 kHz, < 1 ps rms jitter). Quality RF Test equipment may be used as a sample clock source as long as it meets the Model 361 sample clock frequency and power requirements.



The SNR of high frequency signals ($F_{in} > 100$ MHz) can be improved by using an external sample clock with better phase noise than that of the internal synthesizer.

The user supplied external clock waveform may be a sinusoid or square wave as long as the phase noise/jitter characteristic is low. Sine wave inputs should operate at the high end of the permissible input power range to maximize the voltage slope into the ADC clock circuitry. Square wave inputs may be driven at a lower power level since they already have a steep voltage slope.



The user supplied external sample clock may be sinusoidal or square in nature so long as it possesses a low phase noise/jitter characteristic.

5.3.1.2 External Reference Clock

The on-board frequency synthesizer can be phase locked to an external 10 MHz system reference to achieve system-wide phase coherence by simply connecting a source to the reference/clock SMA. The AC power level on the reference input is continuously monitored to automatically detect the presence of an external source. If the power level exceeds the established threshold, the internal TCXO power is automatically turned off. There is hysteresis built into the detection circuit to prevent oscillation around the threshold. Only a high quality low phase noise (< -145 dBc/Hz @ 10 kHz) source should be used as an external reference. External reference source harmonic content above 50 MHz exceeding a level of -10 dBm will cause the external clock detector to trip and supply the wrong sample clock. Clock input level requirements can be found in section 3.3.



Generally the synthesized output of an RF signal generator should not be used as a 10 MHz reference source due to high phase noise. Most generators feature a separate dedicated low phase noise 10 MHz reference output that should be used instead.



The spectral power level of the external reference source above 50 MHz must be less than -10 dBm.

5.3.2 ADC Clock Distribution

A block diagram illustrating the data and clock paths for the receiver is shown in Figure 5-8. The ADC data from the receiver is registered into the FPGA using a copy of the sample clock. Data timing is adjusted automatically using the IDELAY features of the FPGA. Further information is available in the *Channel Express FPGA Core Manual*.

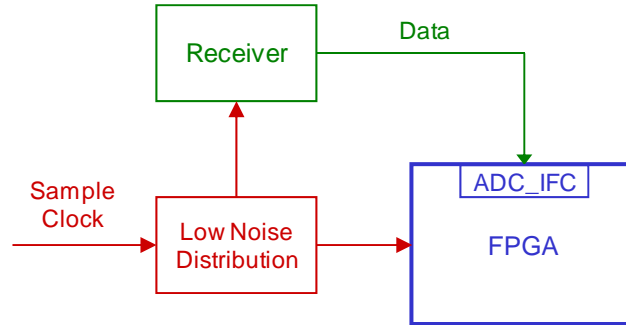


Figure 5-8 Receiver Data Clocking

5.4 SRAM (Build Option)

The Channel Express card can be ordered with an optional four banks of 250 MHz QDR II SRAM yielding an additional 32 Mbytes of storage external to the FPGA as shown in Figure 5-9. Each SRAM block represents a single QDR II SRAM device. The chip is organized as 4M x 18 bits, but only 16 bits of input and output are wired to the FPGA due to the limited number of pins available. The user interface to each SRAM is organized as 2M x 32 bits to ease the timing constraints on the application logic. More information about the SRAM can be found through the vendor data sheet associated with the device. Vendor name and device part number can be found in Table 5-4.

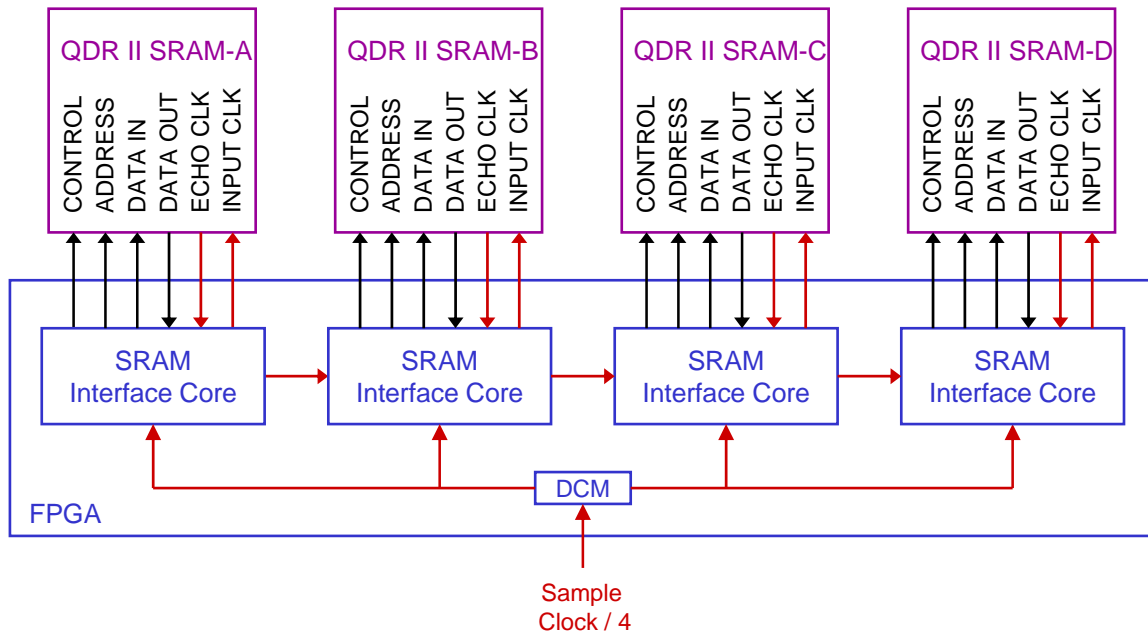


Figure 5-9 External SRAM Interconnect

The SRAM will not operate correctly if the input clock period is outside the range of 4.0 ns to 8.4 ns.

There is a delay-locked loop (DLL) internal to each SRAM that operates over a limited range of input frequencies (119 MHz to 250 MHz). A DCM inside the FPGA can be used to multiply the sample clock to meet the SRAM frequency range requirement.

The SRAM interface core in the FPGA manages the clock domain crossing between data collected at the sample rate and the SRAM running at an integer multiple of this value.

Even if the sample and SRAM clock frequencies are matched, a single SRAM can continuously store data from two input channels since both the read and write ports operate at double data rate.

The SRAM interface FPGA core simplifies user interaction with the memory by managing all of the critical timing, including a self-calibration procedure that runs each time the hardware is reset. Please see the *Channel Express FPGA Core Manual* for more information.

5.5 IO

A block diagram of the Model 361 IO interface is shown in Figure 5-10. There are five user ports connected to the FPGA in addition to a number of LED indicators. The following paragraphs provide a summary of the IO functions found on the Model 361. IO connector details can be found in the external interface description of section 6.0.

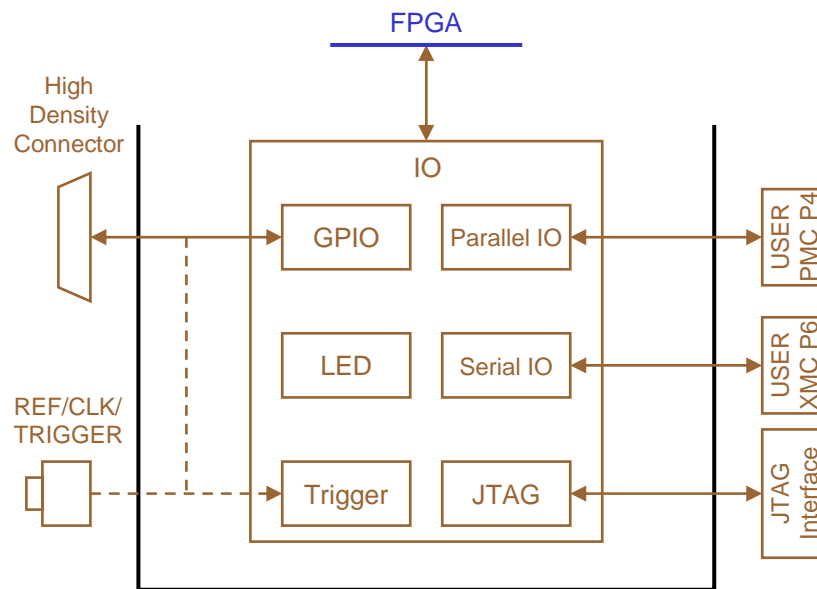


Figure 5-10 IO Block Diagram

5.5.1 GPIO Interface

The Model 361 includes a 15-pin high density front panel connector for general purpose I/O. There are six digital GPIO signals connected to pins on the FPGA as shown in Figure 5-11. The FPGA I/O voltage (VCCO) of the GPIO bank is tied to 3.3 V in standard configurations and can be tied to 2.5V as a build option.

The GPIO pins may use any of the FPGA protocols subject to the IOB and VCCO constraints listed in the Xilinx data sheet. See the FPGA data sheet for IO level and switching characteristics. FPGA part number information can be found in Table 5-4.

There are no terminations external to the FPGA, the only mechanism for termination are the built-in features of the Xilinx IOB. All lines are routed as 50 Ohm differential pairs and length matched to within 1 inch. The GPIO path contains a FET buffer to provide 5 V tolerance and provide FPGA protection. The buffer may be bypassed with zero Ohm resistors as a build option.

! Users must ensure that system IO levels do not exceed FPGA I/O bank voltage maximums. Failure to do so may result in severe FPGA damage.

Two GPIO connections are dedicated to the system monitor ADC built into the FPGA. See section 5.1.1 for more information on system monitor.

One GPIO input is dedicated to a 50 Ohm terminated trigger. This input feeds directly to the FPGA and is not protected by a buffer.

Auxiliary 3.3V or 5.0V DC power is also available from the GPIO Bi-Lobe connector as a build option.

☞ The 50 Ohm terminated input trigger and auxiliary power options are mutually exclusive. Only one or the other may be ordered as a build option.

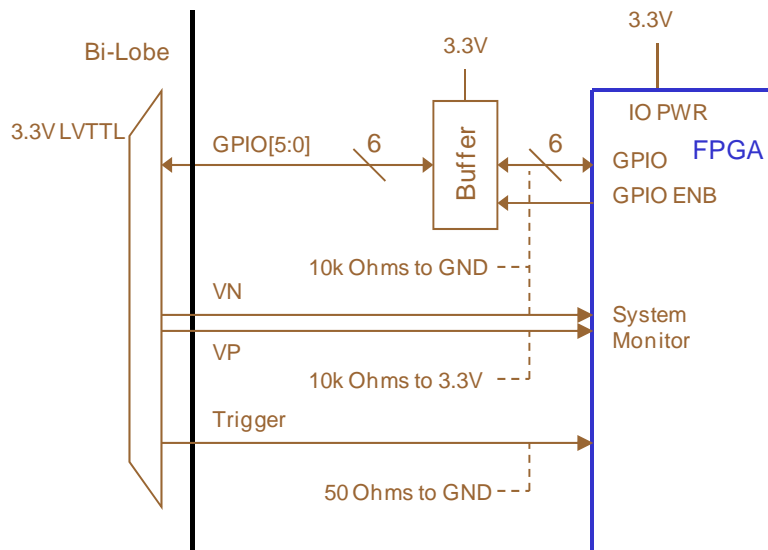


Figure 5-11 GPIO Block Diagram

5.5.2 Coaxial Trigger Interface (Build Option)

The Model 361 contains a coaxial input that can serve as a 50 Ohm terminated LVTTTL external trigger signal as a build option. The input is connected through a single gate 5V tolerant FET buffer directly to the FPGA as shown in Figure 5-12. Trigger input levels are listed in section 3.3. The trigger front panel connection is discussed in section 6.1.

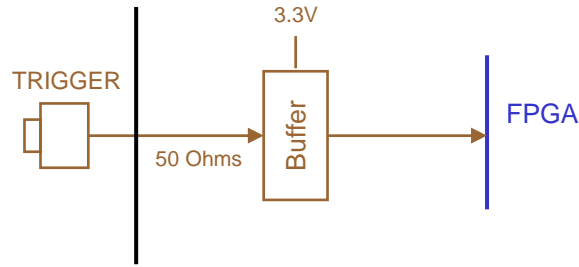



Figure 5-12 Trigger Interface

 Note: the coaxial trigger build option uses the external reference/sample clock connector. An external reference/sample clock cannot be used with the coaxial trigger input build option.

5.5.3 USER IO Interface

There are two user IO ports available for Channel Express as shown in Figure 5-13. The first port consists of FPGA IO routed directly to the legacy PMC P4 connector, the second consists of high-speed serial IO routed directly to the XMC P6 connector. The following paragraphs provide port connectivity details.

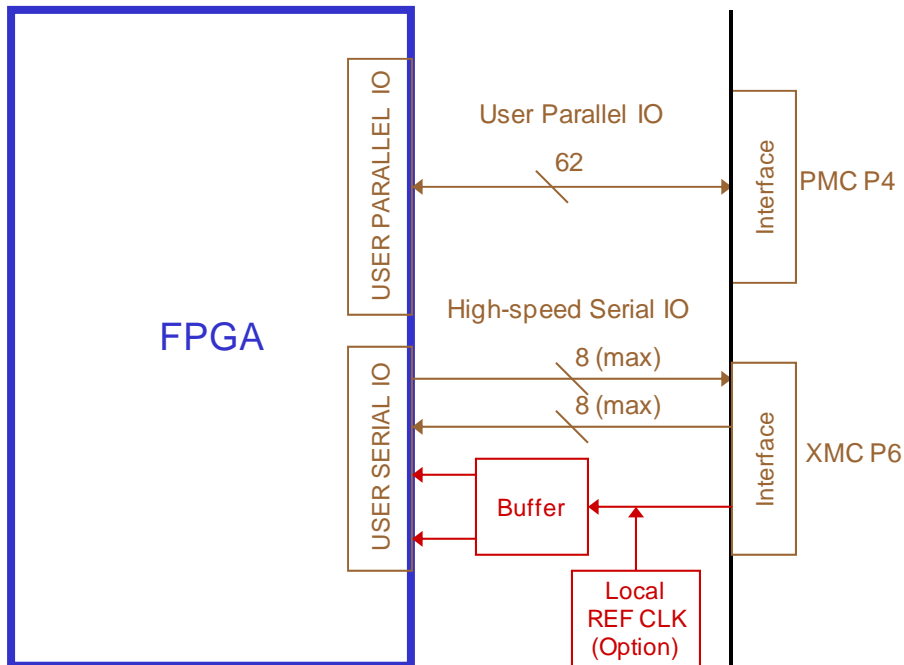


Figure 5-13 User IO Options

5.5.3.1 User Parallel IO (PMC P4)

Channel Express is equipped with a user defined connector that is wired directly to the FPGA user IO interface as shown in Figure 5-14. The FPGA application code can implement any IO standard supported by the FPGA IOB. The FPGA bank voltage (VCCO) must be considered when selecting a standard.

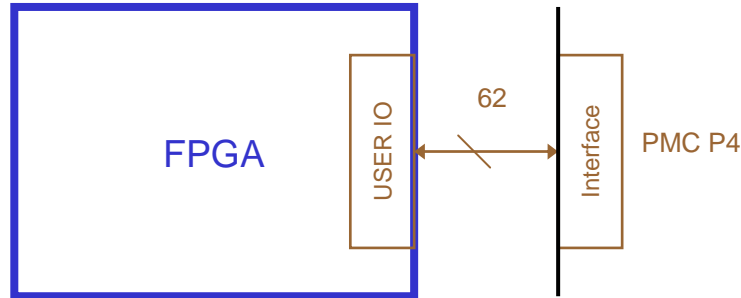


Figure 5-14 USER Parallel IO Interface

The Channel express user parallel IO is wired out as 62 lines arranged as 28 differential pairs plus 6 single ended lines as shown in Figure 5-15. The lines in the differential pairs may also be configured as individual single ended connections. The voltage of the user defined I/O bank can be tied to either 2.5 V (default) or 3.3 V as a build option. Two of the lines (User61/62) are also ac-coupled and back terminated to 50 Ohms prior to connection to clock inputs as shown in Figure 5-16. Users should account for this 50 Ohm load if User lines 61 and 62 are not used as clock inputs. The termination can be removed as a build option.

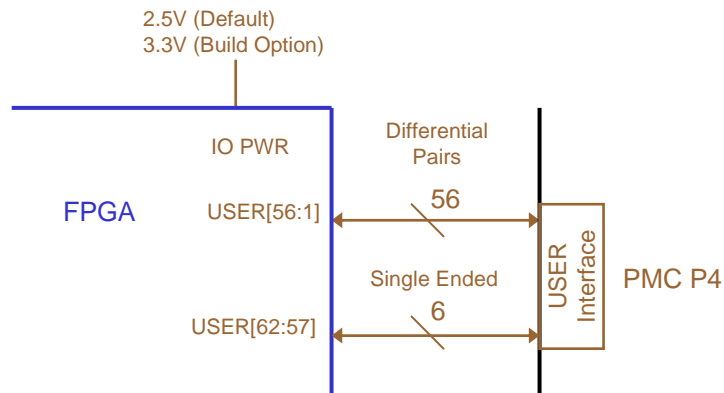


Figure 5-15 USER IO Connections

There are no terminations external to the FPGA, the only mechanism for termination is the DIFF_TERM option in the FPGA IOB. Lines are routed at 50 Ohms nominal impedance and length matched to within 1 inch. See the FPGA data sheet for IO level and switching characteristics. FPGA part number information can be found in Table 5-4. See section 6.3 for connectivity details.

! USER IO is hardwired directly to the FPGA. Users must ensure that system IO levels do not exceed FPGA I/O bank voltage maximums. Failure to do so may result in severe FPGA damage.

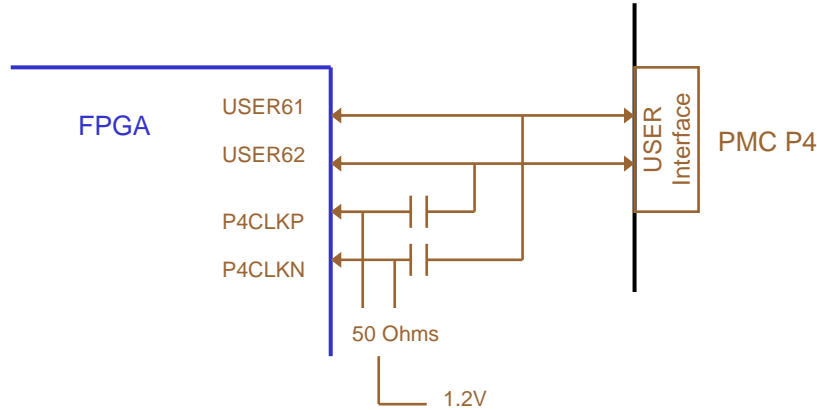


Figure 5-16 Parallel IO Clock Interface

5.5.3.2 High-speed Serial IO (XMC P6)

The Channel Express is equipped with a user defined connector that is wired directly to the FPGA high-speed serial IO interface as shown in Figure 5-17. The user IO interface supports up to eight bidirectional serial channels, the exact number depends on the size of the FPGA. The high-speed serial IO lines are connected to MGT interfaces in the FPGA. See section 6.2 for connection details.

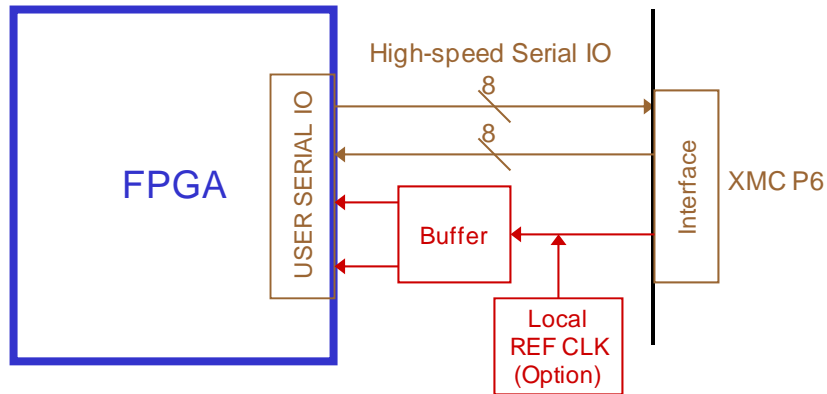


Figure 5-17 USER Serial IO Interface

Channel Express has the facility to operate the serial links from an external reference clock. The clock can be sourced from the XMC P6 connector or from a local source as a build option as shown in Figure 5-18. The buffer is a low voltage CML fanout buffer that serves to split the main clock into two MGT reference clocks, one for each high-speed serial IO bank. Clock level specifications can be found in FPGA vendor data sheet. Clock connectivity information can be found in Table 6-3. Fanout buffer information can be found from the component vendor data sheet referenced in Table 5-4.

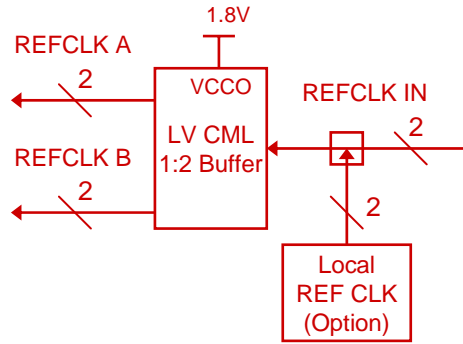


Figure 5-18 USER Serial IO Reference Clock Interface

! USER IO is hardwired directly to the FPGA. Users must ensure that system IO levels do not exceed FPGA I/O bank voltage maximums. Failure to do so may result in severe FPGA damage.

5.5.4 JTAG Interface

The FPGA and Configuration PROM are user programmable devices that can be loaded with application logic directly from the host through a JTAG header. As shown in Figure 5-19, the JTAG chain is composed of the Configuration PROM followed by the FPGA.

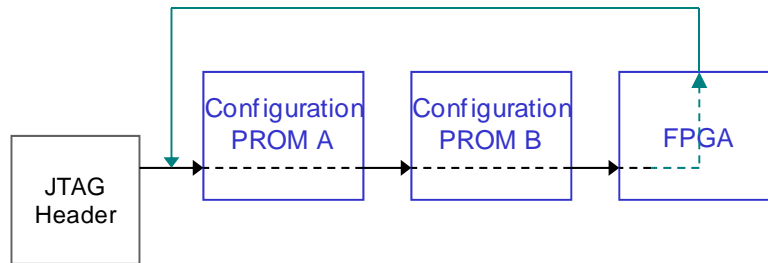


Figure 5-19 JTAG Chain

A JTAG interface header provides access to the Xilinx Configuration PROM and FPGA. The JTAG port can be directly connected to a Xilinx programming cable to configure the devices using the Xilinx iMPACT™ tool or perform debug with Xilinx ChipScope™. See section the *Channel Express FPGA Core Manual* for information on programming the PROM and FPGA via the JTAG port. See section 6.4.1 for JTAG header location and pin descriptions.

5.5.5 LED Indicators

Several LED indicators are available on the Model 361 to provide visual configuration confirmation and support integration and test efforts. A detailed list of LED functions and locations can be found in section 6.4.2 of this document.

5.6 Key Components

The key hardware components for the Model 361 assembly are listed in Table 5-4. This information is supplied to assist in the development of custom application logic for the FPGA.

Table 5-4 Key Hardware Components

Component	Part Number	Vendor	Comments
Receiver ADC	LTC2209	Linear Technology	16-bit, 160 MSPS, A/D Converter
Offset DAC	LTC1661	Linear Technology	Dual 10-bit Micropower DAC
Virtex-5 FPGA	XC5VLX50T XC5VLX85T XC5VLX110T XC5VLX155T XC5VSX50T XC5VSX95T	Xilinx	Virtex-5 FPGA w/serial ports LX: High-performance logic SX: Ultra-high-performance DSP
Config PROM	XCF08P XCF32P	Xilinx	Configuration PROMs for the FPGA, the XCF08P is depopulated for smaller gate count parts. See Xilinx data sheet for more information.
Serial EEPROM	AT24C02BN-SH-B	ATMEL	2kb serial EEPROM used for FRU identification storage.
SRAM (Optional)	K7R641882M-FC25	Samsung	QDR II SRAM, 250 MHz
Single FET Buffer	74CB3T1G125	TI	Single FET bus switch
Octal FET Bus Switch (GPIO Buffer)	74CB3T3245	TI	Octal FET bus switch
LV CML 1:2 Buffer	SY54011RMG	Micrel	Low Voltage 1.2/1.8V CML 1:2 Fanout Buffer, 3.2GHz
Local REF Clock (Optional)	530KB100M000DG	Silicon Labs	OSC CLCC-6 100 MHz 1.8V CML Crystal Oscillator
Low Noise Clock Distribution	AD9512	Analog Devices	1.2 GHz Clock Distribution IC.
Frequency Synth	ASY-817-033	Red Rapids	160 MHz (default) fixed frequency synthesizer.
TCXO	VTC4-A01D-10M000	Vectron	Oscillator, 10 MHz, ± 1.0 ppm
GPIO Connector	A28100-015	Omnetics	15-circuit right-angle Bi-Lobe connector
GPIO Mating Connector	A29000-115	Omnetics	15-circuit Bi-Lobe mating connector with 30" pig tail (30 AWG)

6.0 External Interfaces

6.1 Front Panel Interface

There are four external connectors located along the face of the Model 361 module as shown in Figure 6-1. The three coaxial SMA connectors are 50 Ohm terminated analog inputs. Two of the connectors are assigned to the receiver A/B channel signal inputs and the third serves as an external reference/sample clock input (default) or trigger input (build option). A 15-pin high density connector is also provided for general purpose I/O (GPIO) providing 8 digital signals and one DC power pin.

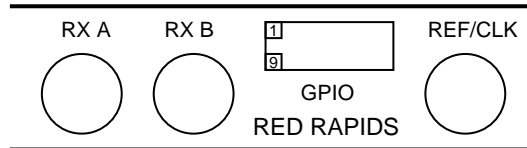


Figure 6-1 Model 361 Front Panel Connectors

Table 6-1 Front Panel Connectors

Des	Label	Connector	Description
J1	RX A	SMA	Receiver Channel A
J2	RX B	SMA	Receiver Channel B
P1	GPIO	High Density 15pin	General Purpose IO
J3	REF/CLK/TRIG	SMA	10 MHz reference/Sample Clock/Trigger

The REF/CLK SMA connector can be configured as an external trigger input as a build option. The trigger input in this case is terminated into 50 Ohms and routed through a 5V tolerant buffer.

Digital GPIO is supplied through an Omnetics Dual Row Bi-Lobe 15-position connector (PN A28100-015). The pinout for the connector is shown in Table 6-2. The FPGA and buffer output drive source voltage for all designated I/O pins is set to 3.3 V. The GPIO pins use 3.3V LVTTTL protocol, voltage levels are listed in section 3.6. The Trigger input is terminated to 50 Ohms on the board.

Inputs to the FPGA System Monitor ADC are also supplied through the Omnetics Bi-Lobe connector. Consult the *Xilinx Virtex-5 System Monitor User Guide* for information on the expected input voltage levels.

The mating connector assembly is available from Red Rapids or directly from Omnetics (PN A29000-115). Red Rapids supplies one mating connector cable assembly with each unit. The cable assembly consists of a single mating connector and an 18 inch minimum pigtail. Connector details are shown in Figure 6-3 and Figure 6-3.

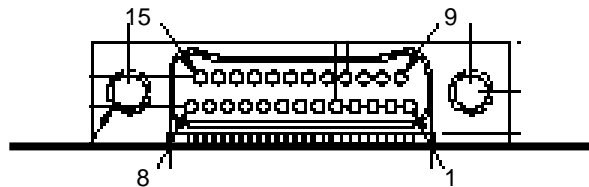


Figure 6-2 General Purpose I/O Connector Detail

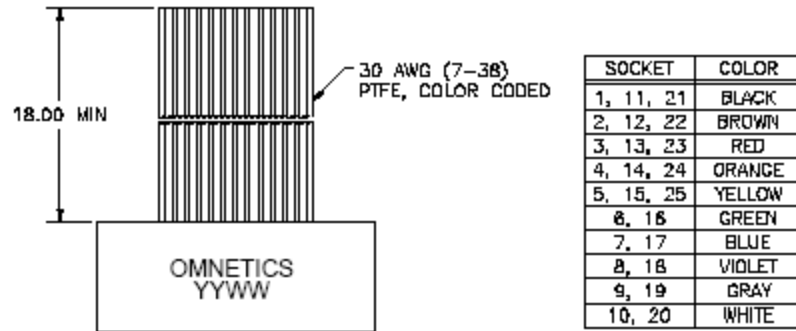


Figure 6-3 General Purpose I/O Mating Cable Connector

Table 6-2 General Purpose I/O Connector Pinout

Pin	Signal Type	Signal Name
1	GND	N/A
2	GND	N/A
3	GND	N/A
4	GND	N/A
5	GND	N/A
6	GND	N/A
7	Input (50 Ohm)	Trigger
8	System Monitor ADC	VP
9	I/O	GPIO1
10	I/O	GPIO2
11	I/O	GPIO3
12	I/O	GPIO4
13	I/O	GPIO5
14	I/O	GPIO6
15	System Monitor ADC	VN

6.2 Host Interface

The host interface for Channel express card is the PCI Express (PCIe) bus. The location and pin assignments for the PCIe bus host connector (P5) are dictated by the XMC PCI Express specification. FPGA pin assignments can be found in the FPGA Development Kit UCF supplied with the unit.

6.3 User IO

Channel Express features two user IO interfaces. The user parallel IO interface consists of 62 lines routed between the FPGA and the PMC P4 connector. The user serial IO interface consists of eight bidirectional high-speed differential pairs plus clock routed between the FPGA and the XMC P6 connector. The following sections provide connector pin information.

6.3.1 *Parallel User IO (PMC P4)*

The PMC P4 connector pin assignments are listed in Table 6-3. FPGA pin assignments can be found in the UCF file provided with the FPGA development kit download. A description of the user parallel IO interface can be found in section 5.5.3.1.

Table 6-3 PMC P4 User Defined Connector Pinout

Name	P4 Pin	P4 Pin	Name
USER1(N1)	1	2	USER2(N2)
USER3(P1)	3	4	USER4(P2)
USER5(N3)	5	6	USER6(N4)
USER7(P3)	7	8	USER8(P4)
USER9(N5)	9	10	USER10(N6)
USER11(P5)	11	12	USER12(P6)
USER13(N7)	13	14	USER14(N8)
USER15(P7)	15	16	USER16(P8)
USER17(N9)	17	18	USER18(N10)
USER19(P9)	19	20	USER20(P10)
USER21(N11)	21	22	USER22(N12)
USER23(P11)	23	24	USER24(P12)
USER25(N13)	25	26	USER26(N14)
USER27(P13)	27	28	USER28(P14)
USER29(N15)	29	30	USER30(N16)
USER31(P15)	31	32	USER32(P16)
USER33(N17)	33	34	USER34(N18)
USER35(P17)	35	36	USER36(P18)
USER37(N19)	37	38	USER38(N20)
USER39(P19)	39	40	USER40(P20)
USER41(N21)	41	42	USER42(N22)
USER43(P21)	43	44	USER44(P22)
USER45(N23)	45	46	USER46(N24)
USER47(P23)	47	48	USER48(P24)
USER49(N25)	49	50	USER50(N26)
USER51(P25)	51	52	USER52(P26)
USER53(N27)	53	54	USER54(N28)
USER55(P27)	55	56	USER56(P28)
USER57	57	58	USER58
USER59	59	60	USER60
USER61 ⁽¹⁾	61	62	USER62 ⁽¹⁾
NC	63	64	NC

Notes:

- (1) Pins highlighted in yellow are ac-coupled and back terminated into 50 Ohms, see Figure 5-16 for more information.

6.3.2 Serial User IO (XMC P6)

The XMC P6 connector pin assignments are listed in Table 6-4. FPGA pin assignments can be found in the UCF file provided with the FPGA development kit download. A description of the user serial IO interface can be found in section 5.5.3.2.

Table 6-4 User Serial IO Pin Connections

	A	B	C	D	E	F
01	TXSIOp0	TXSIOn0	NC	TXSIOp1	TXSIOn1	NC
02	GND	GND	NC	GND	GND	NC
03	TXSIOp2	TXSIOn2	NC	TXSIOp3	TXSIOn3	NC
04	GND	GND	NC	GND	GND	NC
05	TXSIOp4	TXSIOn4	NC	TXSIOp5	TXSIOn5	NC
06	GND	GND	NC	GND	GND	NC
07	TXSIOp6	TXSIOn6	NC	TXSIOp7	TXSIOn7	NC
08	GND	GND	NC	GND	GND	NC
09	NC	NC	NC	NC	NC	NC
10	GND	GND	NC	GND	GND	NC
11	RXSIOp0	RXSIOn0	NC	RXSIOp1	RXSIOn1	NC
12	GND	GND	NC	GND	GND	NC
13	RXSIOp2	RXSIOn2	NC	RXSIOp3	RXSIOn3	NC
14	GND	GND	NC	GND	GND	NC
15	RXSIOp4	RXSIOn4	NC	RXSIOp5	RXSIOn5	NC
16	GND	GND	NC	GND	GND	NC
17	RXSIOp6	RXSIOn6	NC	RXSIOp7	RXSIOn7	NC
18	GND	GND	NC	GND	GND	NC
19	SIREFCLKP	SIREFCLKN	NC	NC	NC	NC

6.4 Board Interface

6.4.1 JTAG Interface

Figure 6-4 illustrates a typical location of the JTAG connector on the back of the Channel Express product. The header consists of six recessed pin receptacles spaced on 0.1 inch centers. The receptacle will accept a 0.022 inch to 0.034 inch diameter pin or a 0.025 inch square pin. The flying leads supplied with the Xilinx programming cable are compatible with the receptacles. All of the pins except TRSTB must be connected for programming.

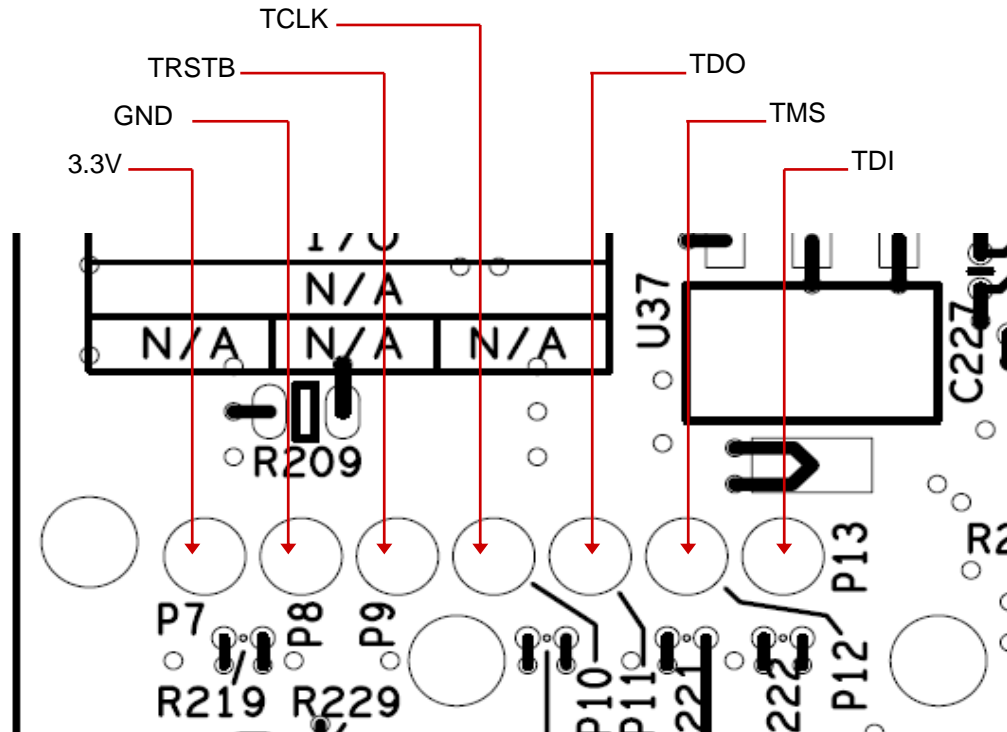


Figure 6-4 JTAG Header

Table 6-5 lists the mapping of pin reference designators on the PWB to the corresponding JTAG signal name.

Table 6-5 JTAG Header Signal Mapping

Reference Designator	Signal Name
P7	3.3V
P8	GND
P9	TRSTB
P10	TCLK
P11	TDO
P12	TMS
P13	TDI

6.4.2 PMC LED Indicators

There are several LED indicators that report various hardware status functions as listed in Table 6-6. Two of the LEDs (D6 & D7) are tied to a bit in the *LED Control* register which can be toggled from application software.

Table 6-6 LED Operating Status Indicators

Reference Designator	Color	Status (Illuminated)
D1	Yellow	User LED "A" active.
D2	Green	User LED "B" active.
D3	Red	Internal synthesizer fault (not locked).
D4	Yellow	External 10 MHz reference clock active.
D5	Green	Internal 10 MHz reference clock active.
D6	Yellow	External sample clock active.
D7	Green	Internal sample clock active.

The diode locations are shown in Figure 6-5.

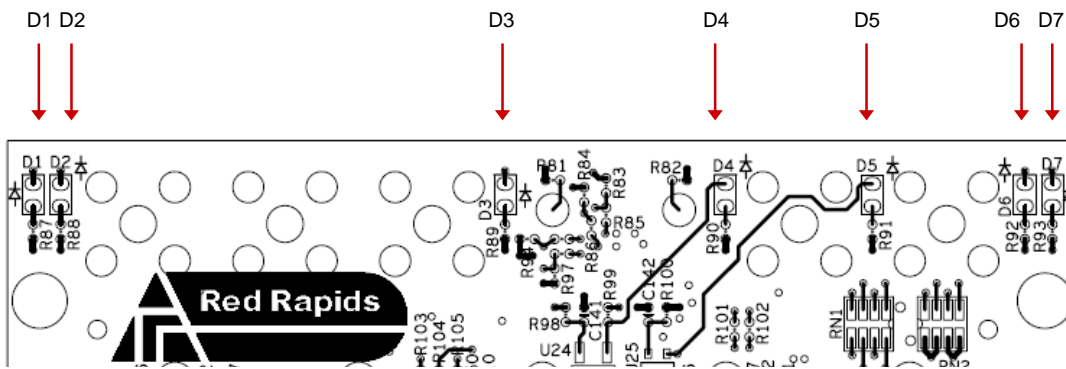


Figure 6-5 Diode Location

7.0 Technical Support

Please feel free to contact us if you have a technical question about or problem with our product. We understand that our customers have tight deadlines and time is of the essence in development and production cycles. We will make every effort to resolve problems as quickly as possible.

Web: www.redrapids.com

Email: support@redrapids.com

Phone: 972-671-9570

Fax: 972-671-9572

Please include the following information with your correspondence:

Contact Information

Product Model

Host Card or System (PC, PCI Carrier, Single Board Computer)

Operating System

Problem Description