Channel Express Reference Design Operating Guide

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1.0 Introduction

1.1 Contents and Structure

This manual describes the features and operation of the reference design supplied with all Channel Express products. It is one component of the complete product documentation suite. Supporting publications are listed in Section 0.

Section	Description
Section 1	Introductory information about the manual.
Section 2	Description of the Receiver, Transmitter, and Transceiver reference designs.
Section 3	Description of the FastApp code used to demonstrate the reference design.
Section 4	Detailed description of the reference design memory map.

The latest product documentation and software is available for download from the Red Rapids website (www.redrapids.com).

1.2 Related Publications

Author	Number	Title
Red Rapids	REF-359-000	Model 359 Hardware Reference Manual
Red Rapids	REF-361-000	Model 361 Hardware Reference Manual
Red Rapids	REF-362-000	Model 362 Hardware Reference Manual
Red Rapids	REF-363-000	Model 363 Hardware Reference Manual
Red Rapids	REF-365-000	Model 365 Hardware Reference Manual
Red Rapids	REF-366-000	Model 366 Hardware Reference Manual
Red Rapids	REF-360-001	Channel Express Installation Guide
Red Rapids	REF-360-003	Channel Express FPGA Core Reference Manual
Red Rapids	REF-806-902	Adapter Device Driver and API Reference Manual
Red Rapids	REF-806-950	FastApp Utility Reference Manual
PCI SIG	PCI Express Base Rev 2.0	PCI-SIG, PCI Express Base Specification Revision 2.0

1.3 Conventions

This manual uses the following conventions:

- Hexadecimal numbers are prefixed by “0x” (e.g. 0x00058C).
- Blue font is used for names of directories, files and OS commands.
- Green font is used to designate source code.
- Active low signals are followed by ‘#’, For example, TRST#.

☞	Text in this format highlights useful or important information.

!	Text shown in this format is a warning. It describes a situation that could potentially damage your equipment. Please read each warning carefully.

The following are some of the acronyms used in this manual.

- **ADC** Analog to Digital Converter
- **BAR** Base Address Register
- **DAC** Digital to Analog Converter
- **DMA** Direct Memory Access
- **ISR** Interrupt Service Routine
- **PCIe** Peripheral Component Interconnect Express

1.4 Manual Compatibility

The applicable hardware part numbers are defined as follows:

- Model 359-XXX *Channel Express RX2 14/500*
- Model 361-XXX *Channel Express RX2 16/160*
- Model 362-XXX *Channel Express XCVR2 16/160*
- Model 363-XXX *Channel Express RX2 14/400*
- Model 365-XXX *Channel Express XCVR2 14/400*
- Model 366-XXX *Channel Express RX2 8/1500*

1.5 Distribution Disk (DSK-360-002-Rxx)

Operation of the Channel Express reference design is demonstrated using the FastApp software utility. The FastScript files required to demonstrate the reference design are distributed on Red Rapids disk archive number DSK-360-002-Rxx. The directory structure of the archive is outlined below:

\alias

The alias subdirectory contains a file of symbolic constants that are specific to the Channel Express reference design memory map.

\express

The express subdirectory contains FastScript command files for each Channel Express product. The file names (Mxxx) match the unique model numbers (Model xxx).

\linux_x86-32

The linux_x86-32 subdirectory contains batch files to run the FastApp utility on a 32-bit Linux distribution hosted on an Intel processor architecture. A Makefile is also included to compile the FastCode source that is produced by the FastApp code generator.

\linux_x86-64

The linux_x86-64 subdirectory contains batch files to run the FastApp utility on a 64-bit Linux distribution hosted on an Intel processor architecture. A Makefile is also included to compile the FastCode source that is produced by the FastApp code generator.

\win_x86-32

The win_x86-32 subdirectory contains batch files to run the FastApp utility on all 32-bit Windows operating systems hosted on an Intel processor architecture. A Visual Studio batch file is also included to compile the FastCode source that is produced by the FastApp code generator.

\win_x86-64

The win_x86-64 subdirectory contains batch files to run the FastApp utility on all 64-bit Windows operating systems hosted on an Intel processor architecture. A Visual Studio batch file is also included to compile the FastCode source that is produced by the FastApp code generator.

1.6 Revision History

Version	Date	Description
R00	12/10/2008	Initial release.
R02	7/5/2011	Major update to reflect the new FastApp utility.
R03	8/8/2011	Address Bar0 0x2000 is write only. Corrected input signal amplitudes for receiver verification test.
R04	10/4/2011	Corrected software distribution disk number.

2.0 Design Description

Each Channel Express product ships with a reference design preloaded in the FPGA PROM. The specific design depends on whether the product is equipped with only ADC channels (Receiver), only DAC channels (Transmitter), or both (Transceiver). These designs demonstrate basic signal acquisition and/or generation using the hardware.

A Xilinx ISE project for each reference design is supplied with the *Chanel Express FPGA Development Kit*.

All of the reference designs are exercised with the FastApp software utility.

2.1 Receiver Reference Design

The Receiver design consists of a single DMA write channel assigned to each ADC. A 32 kbyte FIFO acts as a rate buffer between the ADC and the PCIe interface. Figure 2-1 illustrates a dual channel Receiver datapath from the Channel Express hardware through the host computer. The Receiver supplies data samples to the host in two's complement format. Output files containing raw sample data can be created by writing the contents of each DMA buffer to disk.

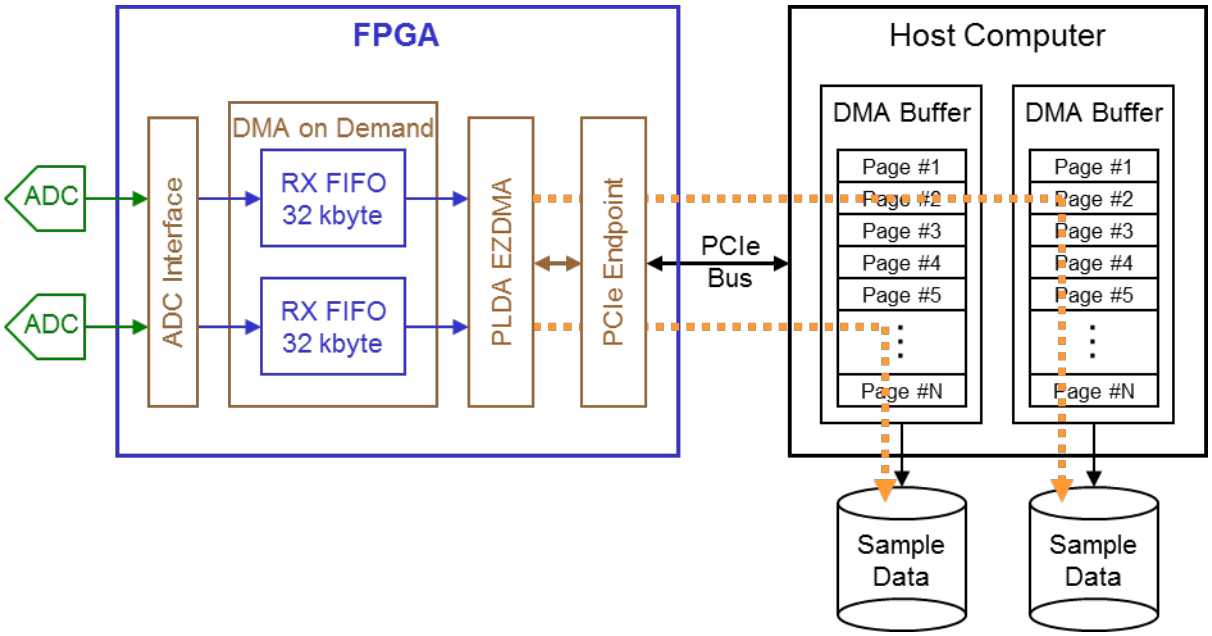

Figure 2-1 Receiver Datapath

The Receiver design supports both snapshot and continuous signal acquisition. The simplest demonstration is a snapshot collection of a single 32 kbyte segment of ADC samples. The entire segment can be captured in the FIFO before initiating a DMA transfer to host memory. The PCIe bus speed is not critical in this case because data can remain in the FIFO for as long as the transfer may take. Once the FIFO is drained, the samples can be copied from the DMA buffer to a file by the application software.

The performance of the PCIe bus must be considered when operating in continuous mode or capturing snapshots greater than 32 kbytes. The sustained bus throughput has to be greater than the composite sample rate from all active ADC channels to prevent a FIFO overflow. Continuously writing data to a file is limited even further by the performance of the disk interface, which is typically much slower than the PCIe bus.

2.1 Transmitter Reference Design

The Transmitter design consists of a single DMA read channel assigned to each DAC. A 32 kbyte FIFO acts as a rate buffer between the PCIe interface and the DAC. Figure 2-2 illustrates a dual channel Transmitter datapath from the host computer through the DAC. The Transmitter accepts data samples from the host in two's complement format. Input files containing raw sample data can be used to refresh the contents of each DMA buffer.

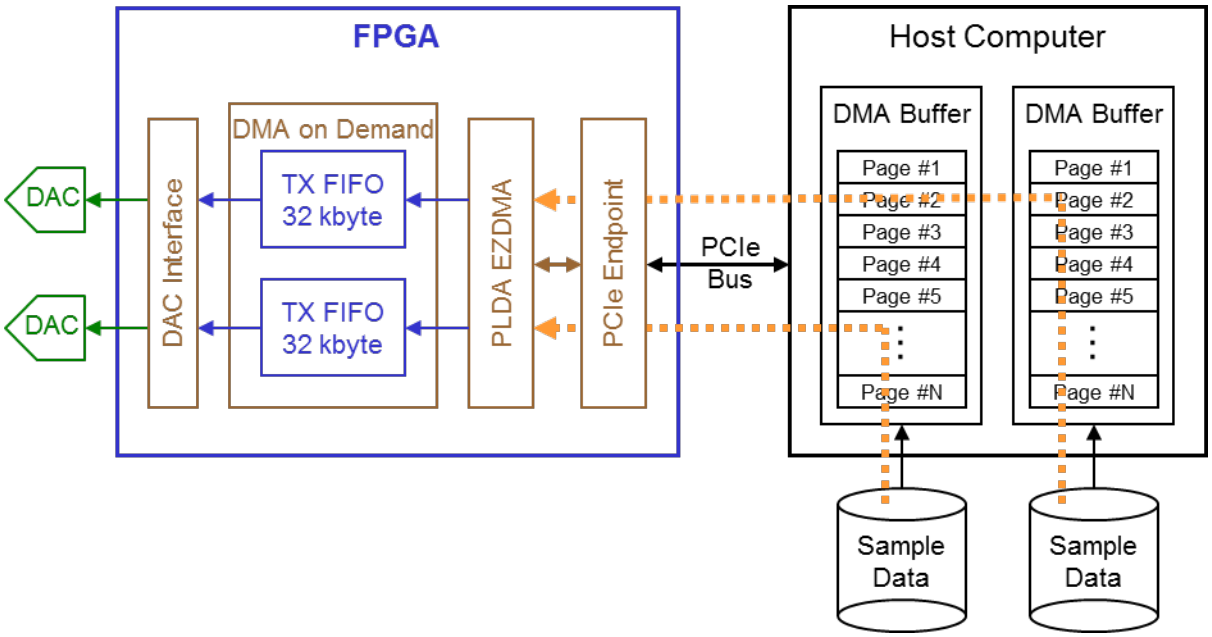

Figure 2-2 Transmitter Datapath

The Transmitter design supports both snapshot and continuous signal generation. The snapshot mode relies on a small segment of fixed sample data pre-stored in the FPGA. These samples represent sixteen points on one period of a sine wave. An analog tone can be created at the output of the DAC by continuously cycling through these samples. The frequency of the tone is software selectable to one quarter, one eighth, or one sixteenth of the DAC sample clock.

The performance of the PCIe bus must be considered when operating in continuous mode. The sustained bus throughput has to be greater than the composite sample rate from all active DAC channels to prevent a FIFO underflow. Continuously reading data from a file is limited even further by the performance of the disk interface, which is typically much slower than the PCIe bus.

2.2 Transceiver Reference Design

The Transceiver design is simply a combination of both the Receiver and Transmitter designs in a single entity.

3.0 Demonstration Code

A single batch file (express) is used to run the FastApp interpreter and the FastApp code generator on all Channel Express reference designs. The batch files are located in the DSK-360-002-Rxx subdirectory that describes the type of operating system running on the host. Refer to Section 1.5 for further details.

FastScript command files are executed by the FastApp interpreter to demonstrate snapshot operation of the receiver and/or transmitter channels. The FastApp code generator also converts these command files to FastCode C language source that can be by compiled into a standalone executable.

Table 3-1 lists the name of the FPGA reference design and the command line input required to execute the batch file for each Channel Express product.

Table 3-1 Reference Design and Command Line Input

Product	FPGA Reference Design	Windows Execution	Linux Execution
Model 359	Transceiver	express M359	./express M359
Model 361	Receiver	express M361	./express M361
Model 362	Transceiver	express M362	./express M362
Model 363	Receiver	express M362	./express M362
Model 365	Transceiver	express M365	./express M365
Model 366	Receiver	express M366	./express M366

The Receiver snapshot demonstration captures 32 kbytes of raw sample data on all ADC channels simultaneously. The data from each channel is stored in a separate disk file (chAout.txt, chBout.txt, etc.).

The Transmitter snapshot demonstration generates a continuous output on all DAC channels simultaneously. The analog signal will have a frequency that is one quarter the ADC/DAC sample clock frequency.

The Transceiver demonstration executes both the Receiver and Transmitter snapshot code.

Section 3.1 describes the test equipment connections required to verify the results produced by the snapshot demonstration. Section 3.2 outlines the procedure to compile the FastCode C language source files that are produced by the code generator.

It is highly recommended that the user successfully execute the verification procedure outlined in Section 3.1 before proceeding with custom FPGA and software development.

3.1 Receiver/Transmitter Verification Test Set

The reference design can be used to verify proper installation of the Channel Express hardware and software. A signal generator and/or spectrum analyzer are the only equipment needed to run the verification, as shown in Figure 3-1.

The signal generator can be connected to multiple inputs simultaneously, or data can be collected on just one input channel with the other inputs left open. There is no need to connect anything to the GPIO connector or any other SMA connectors (clock, reference, trigger, etc.).

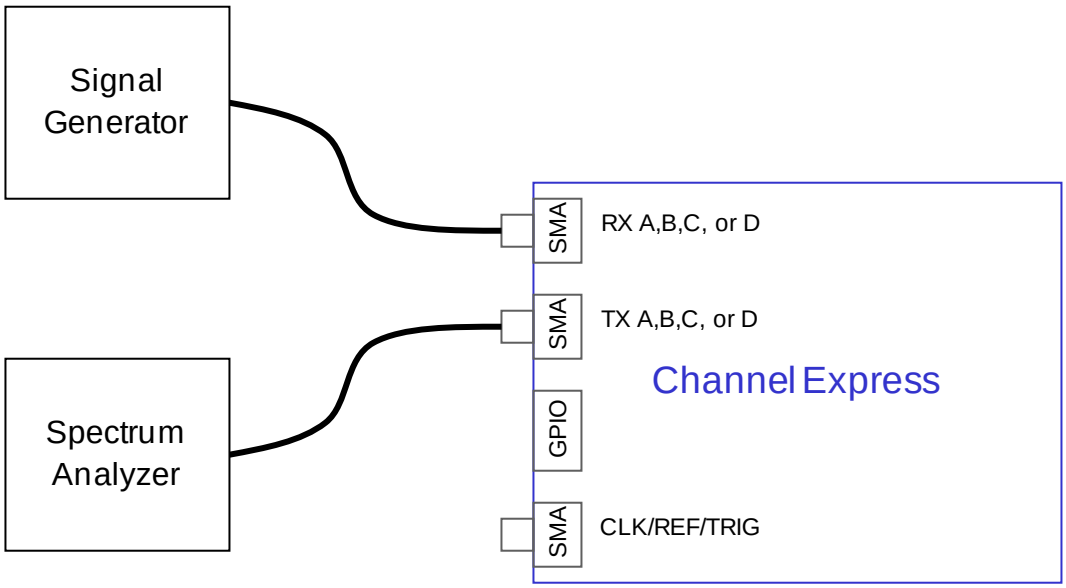

Figure 3-1 Verification Test Set

The input signal amplitude into the receiver will vary with the specific Channel Express product under test. Set the signal generator to produce a 20 MHz sine wave with input power or peak-to-peak voltage listed in Table 3-2. It is also important that the ADC/DAC sample frequency match the value listed in the table. There can be DLL or PLL circuits internal to chips used in the design that need to be programmed for operation over a specific frequency range. The reference designs and corresponding code target the maximum operating frequency supported by the product.

Table 3-2 Input Signal Characteristics

Product	Sample Clock Frequency	Input Signal Frequency	Input Power	Input Voltage
Model 359	500 MHz	20 MHz	+10 dBm	2.0 Vpp
Model 361	160 MHz	20 MHz	+8 dBm	1.6 Vpp
Model 362	160 MHz	20 MHz	+8 dBm	1.6 Vpp
Model 363	400 MHz	20 MHz	+10 dBm	2.0 Vpp
Model 365	400 MHz	20 MHz	+10 dBm	2.0 Vpp
Model 366	1500 MHz	20 MHz	+2 dBm	0.8 Vpp

! Exceeding the recommended input signal power may result in permanent damage to the equipment.

If you purchased a different synthesizer frequency option than listed in Table 3-2, you may need to supply an external sample clock through the front of the card to run the verification test. Consult the *Hardware Reference Manual* for information about the external sample clock characteristics required for each product. The FastScript command file will have to be edited if an external sample clock is supplied. The command line that selects the external clock is commented by default. The comment delimiter can be removed to activate the external clock option.

3.1.1 Receiver Verification

A quick summary of the receiver results can be obtained by simply running the verification software provided with the express software. It is executed from a command prompt on a Linux or Windows platform as follows:

Windows : verify.exe -txt <filename> -bits <ADC> -fs <Fs>

Linux : ./verify -txt <filename> -bits <ADC> -fs <Fs>

where

<filename> = chAout.txt, chBout.txt, etc.

<ADC> = Size of the ADC in bits.

<Fs> = Frequency of the ADC/DAC sample clock in MHz.

The verification software will search for the strongest signal (carrier) and report the output power (dBFS) and frequency (MHz). A properly operating Channel Express will produce an output power between -1 dBFS and -4 dBFS (-3 dBFS nominal) for all models.

The listing below is an example of a verification output report.

```
Red Rapids Spectral Spur Search
Built Oct 31 2006 11:03:49
Opening chAout.txt in txt mode.
Reading from file...
Read 8192 samples from the data file chAout.txt
Will perform a real 8192 point FFT with a bin size of XXX.X Hz over XX.X MHz of
bandwidth
CreateWindow: Entered
Scaling to XX bits, (XXXX)
Applying windowing function
Test Results
Carrier found: -3.370406 dBFS in bin 1311 @ 20.00 MHz from center
```

3.1.2 Transmitter Verification

The continuous wave output from the transmitter can be verified with a spectrum analyzer connected to the DAC output. The continuous wave signal should exhibit an amplitude slightly lower than 0 dBm at a frequency equal to one quarter the ADC/DAC sample clock frequency.

3.2 FastCode Compile

The FastApp code generator will produce three C source code files each time the express batch file is executed:

Mxxx _FastCode.h : Header file that includes definitions for all of the symbols listed in the FastScript alias file.

Mxxx _FastCode.c : Main source code based on the FastScript command file.

RRAdapter_ISR.c : Interrupt service routine code based on the FastScript ISR file. This output file is always required to compile the application, even if no FastScript ISR file was specified.

Note: Mxxx refers to the name of the FastScript command file that was executed.

The FastCode source can be compiled into a standalone application using commercial C language tools. The executable will produce the same behavior as running the FastScript command file through the FastApp interpreter.

3.2.1 Windows

The VSbuild.bat batch file can be executed from any Visual Studio command prompt. Make sure to select the "x64" command prompt for 64-bit operating systems. The target model number must be included in the batch command as follows:

```
VSbuild Mxxx
```

The batch files execute three separate Visual Studio commands to perform the required compile and link tasks:

(1) Compile the application source code (Mxxx _FastCode.c) and the required interrupt service routine source code (RRadapter_ISR.c).

Note: The interrupt service routine is simply a blank stub since this particular application does not generate interrupts.

(2) Link the required interrupt service routine DLL (RRadapter_ISR.dll).

(3) Link the Mxx_FastCode application executable (Mxxx _FastCode.exe).

The output files will be located in a subdirectory named FastCode.

The resulting Mxx_FastCode application can be executed from any Windows command prompt, but the Adapter driver DLL directory must first be included in the path environment variable.

3.2.2 Linux

A Makefile is provided to compile and link the Mxx_FastCode application using gcc. The target model number must be included in the make command as follows:

```
make MODEL=Mxxx
```

The output files will be located in a subdirectory named FastCode.

The resulting Mxx_FastCode application can be executed from any Linux command prompt.

4.0 Memory Map

The Receiver, Transmitter, and Transceiver reference designs use 64-bit aligned addresses on both BAR0 and BAR2. This eliminates BAR1 and BAR3 from the memory map.

BAR0 is typically assigned to the command/status registers that control the various hardware functions on the card while BAR2 is typically assigned to the configuration registers of the application logic. This convention has been maintained in these reference designs.

The memory map is not contiguous, any memory location not called out in the memory map should be considered reserved and should not be accessed. Writing to locations not called out in the memory map may cause erroneous operation.

The following convention is used to describe valid register operations:

(W) Write

(R) Read

(cl) Clear on read

4.1 BAR0 Memory Map

The Channel Express hardware includes several registers that must be initialized either at system power-up or when a software application is opened. Most of the BAR0 register settings remain static, but there may be cases when it is desirable to update a value during normal operation. Some functions also report hardware status through these registers.

The table below summarizes all of the BAR0 registers followed by a more detailed description of each register. A check mark signifies the relevance of each register to a corresponding product number (e.g. Model 365).

Receiver/Transmitter/Transceiver BAR0 Memory Map									
Address Offset (64-bit aligned)	**359**	**360**	**361**	**362**	**363**	**364**	**365**	**366**	**Register Name**
0x0000 - 0x0080			Reserved						Not Defined
0x0088	✓	✓	✓	✓	✓	✓	✓	✓	Interrupt Mask
0x0090 - 0x00E0			Reserved						Not Defined
0x00E8	✓	✓	✓	✓	✓	✓	✓	✓	FPGA Soft Reset
0x00F0 - 0x00F8			Reserved						Not Defined
0x0100	✓	✓	✓	✓	✓	✓	✓	✓	Interrupt Status
0x0108 - 0x0128			Reserved						Not Defined
0x0130	✓	✓	✓	✓	✓	✓	✓	✓	Serial Peripheral Interface (SPI) Bus
0x0138	✓	✓	✓	✓	✓	✓	✓		Chip Resets
0x0140 - 0x01F8			Reserved						Not Defined
0x0200	✓								Model 359 Chip Configuration and Status
		✓							Model 360 Chip Configuration and Status
			✓						Model 361 Chip Configuration and Status
				✓					Model 362 Chip Configuration and Status
					✓				Model 363 Chip Configuration and Status
						✓			Model 364 Chip Configuration and Status
							✓		Model 365 Chip Configuration and Status
								✓	Model 366 Chip Configuration and Status
0x0208 - 0x1EF8			Reserved						Not Defined
0x1F00	✓	✓	✓	✓	✓	✓	✓	✓	DMA Channel 1 and Channel 2 Status
0x1F08	✓	✓	✓	✓	✓	✓	✓	✓	DMA Channel 3 and Channel 4 Status
0x1FF8	✓	✓	✓	✓	✓	✓	✓	✓	Index to DMA Page Addresses and Descriptors (below)
0x2000 - 0x3FF8	✓	✓	✓	✓	✓	✓	✓	✓	DMA Page Addresses and Descriptors

Address	Register Name
0x0088	Interrupt Mask

Product Relevance (checked box)

☒ Model 359 ☒ Model 360 ☒ Model 361 ☒ Model 362
☒ Model 363 ☒ Model 364 ☒ Model 365 ☒ Model 366

Bit(s)	R/W/cl	POR	Function	Description
63:2			Reserved	
1	R/W	0	DMA Interrupt Mask	Logic zero disables all interrupts from the DMA refresh register in BAR2.
0	R/W	0	Error Interrupt Mask	Logic zero disables all interrupts from the error status register in BAR2.

Address	Register Name
0x00E8	FPGA Soft Reset

Product Relevance (checked box)

☒ Model 359 ☒ Model 360 ☒ Model 361 ☒ Model 362
☒ Model 363 ☒ Model 364 ☒ Model 365 ☒ Model 366

Bit(s)	R/W/cl	POR	Function	Description
63:0	W	0	FPGA Soft Reset	Any write transaction to this register, regardless of the data contents, will reset the application logic in the FPGA. The resulting reset operation also clears this register.

Address	Register Name
0x0100	Interrupt Status

Product Relevance (checked box)

☒ Model 359 ☒ Model 360 ☒ Model 361 ☒ Model 362
☒ Model 363 ☒ Model 364 ☒ Model 365 ☒ Model 366

Bit(s)	R/W/cl	POR	Function	Description
63:2			Reserved	
1	R(cl)	0	DMA Interrupt Status	Logic one indicates that the DMA refresh register in BAR2 requires service.
0	R(cl)	0	Error Interrupt Status	Logic one indicates that the error status register in BAR2 requires service.

Address	Register Name
0x0130	Serial Peripheral Interface (SPI) Bus

Product Relevance (checked box)

☒ Model 359 ☒ Model 360 ☒ Model 361 ☒ Model 362
☒ Model 363 ☒ Model 364 ☒ Model 365 ☒ Model 366

Bit(s)	R/W/cl	POR	Function	Description
63:44			Reserved	
43:40	R/W	0x0	Configuration	Code that activates a single chip select (CSN) on the SPI bus. The binary value corresponds to the number assigned to the peripheral, i.e., 0x3 indicates CSN(3).
39:38	R/W	00	Payload Size	Indicates the size in bits of the complete payload (instruction plus data). 00 : 8 bits 01 : 16 bits 10 : 24 bits 11 : 32 bits
37	R/W	0	Clock Edge	Logic one indicates that payload bits will be registered in the peripheral on the rising edge of clock. Logic zero indicates an active falling edge.
36	R/W	0	Start	Logic one initiates a SPI bus transaction.
35:33			Reserved	
32	R	0	Busy	Logic one indicates that the SPI controller is currently busy executing a previous command.
31:0	R/W	0x0	Payload	The payload consists of an instruction word followed by a data word. The length of each word can vary depending on the particular peripheral that is being programmed. The complete payload must be aligned with the LSB and consume as many bits as necessary without gaps. A read operation will return the requested value to this same register aligned with the LSB.

Address	Register Name
0x0138	Chip Resets

Product Relevance (checked box)

☒ Model 359 ☒ Model 360 ☒ Model 361 ☒ Model 362
☒ Model 363 ☒ Model 364 ☒ Model 365 ☐ Model 366

Bit(s)	R/W/cl	POR	Function	Description
63:17			Reserved	
16	R	0	Reset Timer	Logic one indicates that the 64 ns reset timer is active due to any write to this register address. The timer is polled by software to ensure that the minimum reset pulse width is met.
15:4			Reserved	
1	R/W	1	Dual DAC Chip Reset	Logic zero places the dual DAC chip into a reset state.
0	R/W	1	Clock Chip Reset	Logic zero places the sample clock distribution chip into a reset state.

Address	Register Name
0x0200	Model 359 Miscellaneous Configuration and Status

Product Relevance (checked box)

☒ Model 359 ☐ Model 360 ☐ Model 361 ☐ Model 362
☐ Model 363 ☐ Model 364 ☐ Model 365 ☐ Model 366

Bit(s)	R/W/cl	POR	Function	Description
63:19			Reserved	
18	R	UNK	Internal Sample Clock Active	Logic one indicates that the on-board frequency synthesizer is active. The value will be logic zero if an external clock is supplied to the card.
17	R	UNK	Internal Reference Active	Logic one indicates that that on-board reference source (TCXO) is active. The value will be logic zero if an external reference is supplied to the card.
16	R	UNK	Synthesizer Locked	Logic one indicates that the on-board frequency synthesizer is locked to a 10 MHz reference.
15:1			Reserved	
0	R/W	0	Dual DAC SYNC	Logic one synchronizes the dual DAC and enables the output.

Address	Register Name
0x0200	Model 360 Miscellaneous Configuration and Status

Product Relevance (checked box)

☐ Model 359 ☒ Model 360 ☐ Model 361 ☐ Model 362
☐ Model 363 ☐ Model 364 ☐ Model 365 ☐ Model 366

Bit(s)	R/W/cl	POR	Function	Description
31:21			Reserved	
20	R	UNK	Dual DAC PLL_LOCK	Logic one indicates that the PLL internal to the dual DAC is locked.
19	R	UNK	Dual DAC IRQ	Logic zero signals an interrupt request from the Dual DAC. A logic one is expected during normal operation.
18	R	UNK	Internal Sample Clock Active	Logic one indicates that the on-board frequency synthesizer is active. The value will be logic zero if an external clock is supplied to the card.
17	R	UNK	Internal Reference Active	Logic one indicates that that on-board reference source (TCXO) is active. The value will be logic zero if an external reference is supplied to the card.
16	R	UNK	Synthesizer Locked	Logic one indicates that the on-board frequency synthesizer is locked to a 10 MHz reference.
15:7			Reserved	
6	R/W	0	Dual DAC TXENABLE	Logic one enables the dual DAC output.
5:0			Reserved	

Address	Register Name
0x0200	Model 361 Miscellaneous Configuration and Status

Product Relevance (checked box)

☐ Model 359 ☐ Model 360 ☒ Model 361 ☐ Model 362
☐ Model 363 ☐ Model 364 ☐ Model 365 ☐ Model 366

Bit(s)	R/W/cl	POR	Function	Description
31:19			Reserved	
18	R	UNK	Internal Sample Clock Active	Logic one indicates that the on-board frequency synthesizer is active. The value will be logic zero if an external clock is supplied to the card.
17	R	UNK	Internal Reference Active	Logic one indicates that that on-board reference source (TCXO) is active. The value will be logic zero if an external reference is supplied to the card.
16	R	UNK	Synthesizer Locked	Logic one indicates that the on-board frequency synthesizer is locked to a 10 MHz reference.
15:6			Reserved	
5	R/W	0	ADC B PGA	Logic zero selects the high input voltage range to ADC B and logic one selects the low range.
4	R/W	0	ADC A PGA	Logic zero selects the high input voltage range to ADC A and logic one selects the low range.
3	R/W	0	ADC B RAND	Logic zero results in normal operation. Logic one causes ADC B output bits D1-D15 to be EXCLUSIVE-ORed with bit D0.
2	R/W	0	ADC A RAND	Logic zero results in normal operation. Logic one causes ADC A output bits D1-D15 to be EXCLUSIVE-ORed with bit D0.
1	R/W	0	ADC B DITH	Logic zero disables internal dither to ADC B, logic one enables internal dither.
0	R/W	0	ADC A DITH	Logic zero disables internal dither to ADC A, logic one enables internal dither.

Address	Register Name
0x0200	Model 362 Miscellaneous Configuration and Status

Product Relevance (checked box)

☐ Model 359 ☐ Model 360 ☐ Model 361 ☒ Model 362
☐ Model 363 ☐ Model 364 ☐ Model 365 ☐ Model 366

Bit(s)	R/W/cl	POR	Function	Description
31:21			Reserved	
20	R	UNK	Dual DAC PLL_LOCK	Logic one indicates that the PLL internal to the dual DAC is locked.
19	R	UNK	Dual DAC IRQ	Logic zero signals an interrupt request from the Dual DAC. A logic one is expected during normal operation.
18	R	UNK	Internal Sample Clock Active	Logic one indicates that the on-board frequency synthesizer is active. The value will be logic zero if an external clock is supplied to the card.
17	R	UNK	Internal Reference Active	Logic one indicates that that on-board reference source (TCXO) is active. The value will be logic zero if an external reference is supplied to the card.
16	R	UNK	Synthesizer Locked	Logic one indicates that the on-board frequency synthesizer is locked to a 10 MHz reference.
15:7			Reserved	
6	R/W	0	Dual DAC TXENABLE	Logic one enables the dual DAC output.
5	R/W	0	ADC B PGA	Logic zero selects the high input voltage range to ADC B and logic one selects the low range.
4	R/W	0	ADC A PGA	Logic zero selects the high input voltage range to ADC A and logic one selects the low range.
3	R/W	0	ADC B RAND	Logic zero results in normal operation. Logic one causes ADC B output bits D1-D15 to be EXCLUSIVE-ORed with bit D0.
2	R/W	0	ADC A RAND	Logic zero results in normal operation. Logic one causes ADC A output bits D1-D15 to be EXCLUSIVE-ORed with bit D0.
1	R/W	0	ADC B DITH	Logic zero disables internal dither to ADC B, logic one enables internal dither.
0	R/W	0	ADC A DITH	Logic zero disables internal dither to ADC A, logic one enables internal dither.

Address	Register Name
0x0200	Model 363 Miscellaneous Configuration and Status

Product Relevance (checked box)

☐ Model 359 ☐ Model 360 ☐ Model 361 ☐ Model 362
☒ Model 363 ☐ Model 364 ☐ Model 365 ☐ Model 366

Bit(s)	R/W/cl	POR	Function	Description
63:19			Reserved	
18	R	UNK	Internal Sample Clock Active	Logic one indicates that the on-board frequency synthesizer is active. The value will be logic zero if an external clock is supplied to the card.
17	R	UNK	Internal Reference Active	Logic one indicates that that on-board reference source (TCXO) is active. The value will be logic zero if an external reference is supplied to the card.
16	R	UNK	Synthesizer Locked	Logic one indicates that the on-board frequency synthesizer is locked to a 10 MHz reference.
15:0			Reserved	

Address	Register Name
0x0200	Model 364 Miscellaneous Configuration and Status

Product Relevance (checked box)

☐ Model 359 ☐ Model 360 ☐ Model 361 ☐ Model 362
☐ Model 363 ☒ Model 364 ☐ Model 365 ☐ Model 366

Bit(s)	R/W/cl	POR	Function	Description
63:19			Reserved	
18	R	UNK	Internal Sample Clock Active	Logic one indicates that the on-board frequency synthesizer is active. The value will be logic zero if an external clock is supplied to the card.
17	R	UNK	Internal Reference Active	Logic one indicates that that on-board reference source (TCXO) is active. The value will be logic zero if an external reference is supplied to the card.
16	R	UNK	Synthesizer Locked	Logic one indicates that the on-board frequency synthesizer is locked to a 10 MHz reference.
15:1			Reserved	
0	R/W	0	Dual DAC SYNC	Logic one synchronizes the dual DAC and enables the output.

Address	Register Name
0x0200	Model 365 Miscellaneous Configuration and Status

Product Relevance (checked box)

☐ Model 359 ☐ Model 360 ☐ Model 361 ☐ Model 362
☐ Model 363 ☐ Model 364 ☒ Model 365 ☐ Model 366

Bit(s)	R/W/cl	POR	Function	Description
63:19			Reserved	
18	R	UNK	Internal Sample Clock Active	Logic one indicates that the on-board frequency synthesizer is active. The value will be logic zero if an external clock is supplied to the card.
17	R	UNK	Internal Reference Active	Logic one indicates that that on-board reference source (TCXO) is active. The value will be logic zero if an external reference is supplied to the card.
16	R	UNK	Synthesizer Locked	Logic one indicates that the on-board frequency synthesizer is locked to a 10 MHz reference.
15:1			Reserved	
0	R/W	0	Dual DAC SYNC	Logic one synchronizes the dual DAC and enables the output.

Address	Register Name
0x0200	Model 366 Miscellaneous Configuration and Status

Product Relevance (checked box)

☐ Model 359 ☐ Model 360 ☐ Model 361 ☐ Model 362
☐ Model 363 ☐ Model 364 ☐ Model 365 ☒ Model 366

Bit(s)	R/W/cl	POR	Function	Description
63:20			Reserved	
19	R	UNK	Dual ADC CalRun	Logic one indicates that an ADC calibration cycle is active.
18	R	UNK	Internal Sample Clock Active	Logic one indicates that the on-board frequency synthesizer is active. The value will be logic zero if an external clock is supplied to the card.
17	R	UNK	Internal Reference Active	Logic one indicates that that on-board reference source (TCXO) is active. The value will be logic zero if an external reference is supplied to the card.
16	R	UNK	Synthesizer Locked	Logic one indicates that the on-board frequency synthesizer is locked to a 10 MHz reference.
15:1			Reserved	
0	R/W	0	Dual ADC CAL	Logic one initiates an ADC calibration cycle. Note: A timer is implemented in the FPGA design to guarantee the minimum 1280 clock period pulse width.

Address	Register Name
0x1F00	DMA Channel 1 and Channel 2 Status

Product Relevance (checked box)

☒ Model 359 ☒ Model 360 ☒ Model 361 ☒ Model 362
☒ Model 363 ☒ Model 364 ☒ Model 365 ☒ Model 366

Bit(s)	R/W/cl	POR	Function	Description
63:48	R/W	0x0	Channel 2 Current Burst	Last burst completed by DMA Channel 2 in the open page. A binary value of zero indicates that there has been no activity in the open page.
47:42			Reserved	
41:32	R/W	0x0	Channel 2 Current Page	Page number currently open by DMA Channel 2. The page numbering is zero based, so the first page will display a binary value of zero.
31:16	R/W	0x0	Channel 1 Current Burst	Last burst completed by DMA Channel 1 in the open page. A binary value of zero indicates that there has been no activity in the open page.
15:10			Reserved	
9:0	R/W	0x0	Channel 1 Current Page	Page number currently open by DMA Channel 1. The page numbering is zero based, so the first page will display a binary value of zero.

Address	Register Name
0x1F08	DMA Channel 3 and Channel 4 Status

Product Relevance (checked box)

☒ Model 359 ☒ Model 360 ☒ Model 361 ☒ Model 362
☒ Model 363 ☒ Model 364 ☒ Model 365 ☒ Model 366

Bit(s)	R/W/cl	POR	Function	Description
63:48	R/W	0x0	Channel 2 Current Burst	Last burst completed by DMA Channel 4 in the open page. A binary value of zero indicates that there has been no activity in the open page.
47:42			Reserved	
41:32	R/W	0x0	Channel 2 Current Page	Page number currently open by DMA Channel 4. The page numbering is zero based, so the first page will display a binary value of zero.
31:16	R/W	0x0	Channel 1 Current Burst	Last burst completed by DMA Channel 3 in the open page. A binary value of zero indicates that there has been no activity in the open page.
15:10			Reserved	
9:0	R/W	0x0	Channel 1 Current Page	Page number currently open by DMA Channel 3. The page numbering is zero based, so the first page will display a binary value of zero.

Address	Register Name
0x1FF8	Index to DMA Page Addresses and Descriptors

Product Relevance (checked box)

☒ Model 359 ☒ Model 360 ☒ Model 361 ☒ Model 362
☒ Model 363 ☒ Model 364 ☒ Model 365 ☒ Model 366

Bit(s)	R/W/cl	POR	Function	Description
63:16			Reserved	
15:0	R/W	0x0	DMA Page Address and Descriptor Index	Each DMA channel can access up to 1024 pages in physical memory of the host computer. Each page is assigned a starting address by the operating system that must be stored on the Channel Express card. All of the DMA channels use the same BAR0 address range to store the 1024 host addresses (0x2000 to 0x3FF8). Each DMA page has a corresponding descriptor that conveys the parameters of that page. There is unique descriptor for each page, which results in up to 1024 descriptors per DMA channel. These descriptors are also stored on the Channel Express card using the same BAR0 address range (0x2000 to 0x3FF8). This register acts as an index into the shared BAR0 address range (0x2000 to 0x3FF8). The following is a list of all valid index values: 0x0000: Nothing selected. 0x0002: Channel 1 DMA page address select. 0x0004: Channel 2 DMA page address select. 0x0008: Channel 3 DMA page address select. 0x0010: Channel 4 DMA page address select. 0x0200: Channel 1 DMA descriptor select. 0x0400: Channel 2 DMA descriptor select. 0x0800: Channel 3 DMA descriptor select. 0x1000: Channel 4 DMA descriptor select. Note: Only a single bit of this register should ever be set to a logic one.

Start Address	End Address	Register Group Name
0x2000	0x3FF8	DMA Page Addresses and Descriptors

Note: This address range is used to store page addresses and descriptors for all of the DMA channels. An index at BAR0 address 0x1FF8 is used to select which specific channel and data type is active.

Product Relevance (checked box)

☒ Model 359 ☒ Model 360 ☒ Model 361 ☒ Model 362
☒ Model 363 ☒ Model 364 ☒ Model 365 ☒ Model 366

Bit(s)	R/W/cl	POR	Function	Description
63:0	W	0x0	Page Address	Physical starting address of DMA page in host memory. There is one descriptor (below) associated with each page, they are linked by sharing this BAR0 address.

Bit(s)	R/W/cl	POR	Function	Description
63:32			Reserved	
31	W	0	Descriptor (Interrupt)	Logic one will cause an interrupt to be issued when the DMA engine has completed servicing the corresponding page. This technique is used to inform the application software of DMA progress.
30	W	0	Descriptor (Last Page)	Set this bit to logic one for the last page in the DMA chain. The application software is not required to use all of the available 1024 pages.
29:16	W	0x0	Descriptor (Burst Size)	Size of each DMA burst, in bytes, for the corresponding page. This value must be a multiple of 8 to maintain 64-bit alignment (8 bytes). Page Size (bytes) = Burst Size x Burst Count
15:0	W	0x0	Descriptor (Burst Count)	Number of bursts assigned to the corresponding DMA page. A value of zero may be used to insert a dummy page that simply issues an interrupt (bit 31). Page Size (bytes) = Burst Size x Burst Count

4.2 BAR2 DMA Memory Map

The BAR2 memory map includes control and status registers related to snapshot and continuous mode operation. The table below summarizes all of the BAR2 registers followed by a more detailed description of each register.

Receiver/Transmitter/Transceiver BAR2 DMA Memory Map	
Byte Address Offset	**Register (Group) Name**
0x0000	Reserved
0x0008	DMA Refresh Interrupt Mask
0x0010	DMA Refresh Status
0x0018-0x07F8	Reserved
0x0800	Revision Code
0x0808	Error Interrupt Mask
0x0810	Error Status
0x0818	Channel Controls
0x0820	Watchdog Status
0x0828	LED Control
0x0830	DAC Sample Rate Divider
0x0838-0xFFF8	Reserved

Address	Register Name
0x0008	DMA Refresh Interrupt Mask

Bit(s)	R/W/cl	POR	Function	Description
63:5			Reserved	
4	R/W	0	Channel 4 Interrupt	A logic zero disables the interrupts that can be generated by a DMA descriptor on Channel 4.
3	R/W	0	Channel 3 Interrupt	A logic zero disables the interrupts that can be generated by a DMA descriptor on Channel 3.
2	R/W	0	Channel 2 Interrupt	A logic zero disables the interrupts that can be generated by a DMA descriptor on Channel 2.
1	R/W	0	Channel 1 Interrupt	A logic zero disables the interrupts that can be generated by a DMA descriptor on Channel 1.
0			Reserved	

Address	Register Name
0x0010	DMA Refresh Status

Bit(s)	R/W/cl	POR	Function	Description
63:5			Reserved	
4	R/cl	0	Channel 4 DMA Complete	Logic one indicates that a DMA descriptor on Channel 4 has signaled the completion of a page operation. This flag is used by software to track DMA refresh status.
3	R/cl	0	Channel 3 DMA Complete	Logic one indicates that a DMA descriptor on Channel 3 has signaled the completion of a page operation. This flag is used by software to track DMA refresh status.
2	R/cl	0	Channel 2 DMA Complete	Logic one indicates that a DMA descriptor on Channel 2 has signaled the completion of a page operation. This flag is used by software to track DMA refresh status.
1	R/cl	0	Channel 1 DMA Complete	Logic one indicates that a DMA descriptor on Channel 1 has signaled the completion of a page operation. This flag is used by software to track DMA refresh status.
0			Reserved	

Address	Register Name
0x0800	Revision Code

Bit(s)	R/W/cl	POR	Function	Description
63:32			Reserved	
31:0	R	Rev	Application Revision Code	Hard-coded constant that indicates the revision level of the FPGA application design. Format: YYYY/MM/DD (i.e. 2010/05/03)

Address		Register Name		
0x0808		Error Interrupt Mask		
Bit(s)	**R/W/cl**	**POR**	**Function**	**Description**
63:17			Reserved	
16	R/W	0	Clock Initialization	Logic zero disables the interrupt that can be generated when the clock initialization function times out before completion.
15			Reserved	
14	R/W	0	Clock Lock	Logic zero disables the interrupt that can be generated when the clock lock function fails to complete.
13	R/W	0	IDELAYCTRL Lock	Logic zero disables the interrupt that can be generated when the IDELAY controller loses lock.
12	R/W	0	Sample Clock DCM Lock	Logic zero disables the interrupt that can be generated when the sample clock DCM loses lock.
11	R/W	0	Channel 4 FIFO	Logic zero disables the interrupt that can be generated by a FIFO overflow (ADC) or underflow (DAC) on DMA Channel 4.
10	R/W	0	Channel 3 FIFO	Logic zero disables the interrupt that can be generated by a FIFO overflow (ADC) or underflow (DAC) on DMA Channel 3.
9	R/W	0	Channel 2 FIFO	Logic zero disables the interrupt that can be generated by a FIFO overflow (ADC) or underflow (DAC) on DMA Channel 2.
8	R/W	0	Channel 1 FIFO	Logic zero disables the interrupt that can be generated by a FIFO overflow (ADC) or underflow (DAC) on DMA Channel 1.
7	R/W	0	Channel 4 ADC/DAC	Logic zero disables the interrupt that can be generated by an ADC or DAC error condition on Channel 4.
6	R/W	0	Channel 3 ADC/DAC	Logic zero disables the interrupt that can be generated by an ADC or DAC error condition on Channel 3.
5	R/W	0	Channel 2 ADC/DAC	Logic zero disables the interrupt that can be generated by an ADC or DAC error condition on Channel 2.
4	R/W	0	Channel 1 ADC/DAC	Logic zero disables the interrupt that can be generated by an ADC or DAC error condition on Channel 1.
3	R/W	0	BAR2 Read Address	Logic zero disables the interrupt that can be generated by a BAR2 slave read address error.
2	R/W	0	BAR2 Write Address	Logic zero disables the interrupt that can be generated by a BAR2 slave write address error.
1	R/W	0	BAR0 Read Address	Logic zero disables the interrupt that can be generated by a BAR0 slave read address error.
0	R/W	0	BAR0 Write Address	Logic zero disables the interrupt that can be generated by a BAR0 slave write address error.

Address		Register Name		
0x0810		Error Status		
Bit(s)	**R/W/cl**	**POR**	**Function**	**Description**
63:17			Reserved	
16	R/cl	0	Clock Initialization	Logic one indicates that the clock initialization function timed out before completion.
15			Reserved	
14	R/cl	0	Clock Lock	Logic one indicates that the clock lock function failed to complete.
13	R/cl	0	IDELAYCTRL Lock	Logic one indicates that the IDELAY controller has lost lock.
12	R/cl	0	Sample Clock DCM Lock	Logic one indicates that the sample clock DCM has lost lock.
11	R/cl	0	Channel 4 FIFO	Logic one indicates that a FIFO overflow (ADC) or underflow (DAC) was detected on DMA Channel 4.
10	R/cl	0	Channel 3 FIFO	Logic one indicates that a FIFO overflow (ADC) or underflow (DAC) was detected on DMA Channel 3.
9	R/cl	0	Channel 2 FIFO	Logic one indicates that a FIFO overflow (ADC) or underflow (DAC) was detected on DMA Channel 2.
8	R/cl	0	Channel 1 FIFO	Logic one indicates that a FIFO overflow (ADC) or underflow (DAC) was detected on DMA Channel 1.
7	R/cl	0	Channel 4 ADC/DAC	Logic one indicates that an ADC or DAC error condition was detected on Channel 4.
6	R/cl	0	Channel 3 ADC/DAC	Logic one indicates that an ADC or DAC error condition was detected on Channel 3.
5	R/cl	0	Channel 2 ADC/DAC	Logic one indicates that an ADC or DAC error condition was detected on Channel 2.
4	R/cl	0	Channel 1 ADC/DAC	Logic one indicates that an ADC or DAC error condition was detected on Channel 1.
3	R/cl	0	BAR2 Read Address	Logic one indicates that a BAR2 slave read address error was detected.
2	R/cl	0	BAR2 Write Address	Logic one indicates that a BAR2 slave write address error was detected.
1	R/cl	0	BAR0 Read Address	Logic one indicates that a BAR0 slave read address error was detected.
0	R/cl	0	BAR0 Write Address	Logic one indicates that a BAR0 slave write address error was detected.

Address		Register Name		
0x0818		Channel Controls		
Bit(s)	**R/W/cl**	**POR**	**Function**	**Description**
63:24			Reserved	
23	R/W	0	Channel 4 Snapshot	Logic one activates Channel 4 snapshot mode.
22	R/W	0	Channel 3 Snapshot	Logic one activates Channel 3 snapshot mode.
21	R/W	0	Channel 2 Snapshot	Logic one activates Channel 2 snapshot mode.
20	R/W	0	Channel 1 Snapshot	Logic one activates Channel 1 snapshot mode.
19	R/W	0	Channel 4 Continuous	Logic one activates Channel 4 continuous mode.
18	R/W	0	Channel 3 Continuous	Logic one activates Channel 3 continuous mode.
17	R/W	0	Channel 2 Continuous	Logic one activates Channel 2 continuous mode.
16	R/W	0	Channel 1 Continuous	Logic one activates Channel 1 continuous mode.
15:9			Reserved	
8	R/W	0	Initialize Clocks	Logic one initializes all of the digital clocks and optimizes I/O timing at any ADC interface.
7	R/W	0	Channel 4 DMA Enable	Logic one enables DMA transfers on Channel 4. Logic zero resets the page address and burst count.
6	R/W	0	Channel 3 DMA Enable	Logic one enables DMA transfers on Channel 3. Logic zero resets the page address and burst count.
5	R/W	0	Channel 2 DMA Enable	Logic one enables DMA transfers on Channel 2. Logic zero resets the page address and burst count.
4	R/W	0	Channel 1 DMA Enable	Logic one enables DMA transfers on Channel 1. Logic zero resets the page address and burst count.
3	R/W	0	Channel 4 FIFO Flush	Logic one flushes the FIFO attached to DMA Channel 4.
2	R/W	0	Channel 3 FIFO Flush	Logic one flushes the FIFO attached to DMA Channel 3.
1	R/W	0	Channel 2 FIFO Flush	Logic one flushes the FIFO attached to DMA Channel 2.
0	R/W	0	Channel 1 FIFO Flush	Logic one flushes the FIFO attached to DMA Channel 1.

Address		Register Name		
0x0820		Watchdog Status		
Bit(s)	**R/W/cl**	**POR**	**Function**	**Description**
63:8			Reserved	
7	R	0	Channel 4 DMA Busy	Logic one indicates that a DMA transaction is in progress on Channel 4.
6	R	0	Channel 3 DMA Busy	Logic one indicates that a DMA transaction is in progress on Channel 3.
5	R	0	Channel 2 DMA Busy	Logic one indicates that a DMA transaction is in progress on Channel 2.
4	R	0	Channel 1 DMA Busy	Logic one indicates that a DMA transaction is in progress on Channel 1.
3:1			Reserved	
0	R	0	Clock Initialization	Logic one indicates that the clock initialization function is busy.

Address		Register Name		
0x0828		LED Control		
Bit(s)	**R/W/cl**	**POR**	**Function**	**Description**
63:4			Reserved	
3:2	R/W	b00	LED B	LED B can be programmed to perform three different functions: b00 Short blink to indicate BAR2 target transaction. b01 Constant illumination. b10 Two second blink derived from the 200 MHz clock. Any other value turns off the LED.
1:0	R/W	b00	LED A	LED A can be programmed to perform three different functions: b00 Short blink to indicate BAR0 target transaction. b01 Constant illumination. b10 Two second blink derived from the PCIe clock. Any other value turns off the LED.

Address	Register Name
0x0830	DAC Sample Rate Divider

Bit(s)	R/W/cl	POR	Function	Description
63:8			Reserved	
7:0	R/W	0x00	Divisor	This register serves two different functions depending on whether a DAC channel is in snapshot or continuous operating mode. In snapshot mode, the divisor will determine the analog output frequency of the DAC as follows: 0x04 Sample clock frequency divided by four. 0x08 Sample clock frequency divided by eight. 0x10 Sample clock frequency divide by sixteen. No other values are allowed. In continuous mode, the divisor will determine how many times each sample value into the DAC will be duplicated. The values allowed are 2, 4, 8, 16, 32, 64, and 128. This feature is needed to rate match the DAC input to the speed of the PCIe bus. Running both DAC channels at 500 Msps requires a sustained PCIe bandwidth of 2 Gbyte/sec. This is beyond the capability of the bus.