Model 150

Wavefront Quadrature Modulator Family

Hardware Reference Manual

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1.0 Introduction

1.1 Contents and Structure

This manual describes the Model 150 PCI Express Quadrature Modulator hardware and in conjunction with the items listed in the supporting documents of section 1.2 provides a complete description of the capabilities and operation of this product. The focus of this manual is the electrical function of the hardware including control structure, signal flow, clock distribution, external interfaces and key components.

The manual is divided into nine sections as follows:

Section	Description
Section 1	Introductory information about the manual.
Section 2	Product overview.
Section 3	Hardware specifications.
Section 4	Absolute maximum conditions without damage.
Section 5	Performance characteristics.
Section 6	Detailed hardware description.
Section 7	External interface descriptions and connector pinouts.
Section 8	Hardware build options
Section 9	Technical support

The latest product documentation and software is available for download from the Red Rapids web site (www.redrapids.com) by following the Technical Support link.

1.2 Supporting Documents

Author	Number	Title
Red Rapids	REF-150-001	Wavefront Modulator Installation Guide
Red Rapids	REF-150-002	Wavefront Modulator Operating Guide
PCI SIG	PCIe Base Spec 2.0	PCI Express Base Specification Revision 2.0
PCI SIG	PCIe CEM Spec 2.0	PCI Express Card Electromechanical Specification Revision 2.0

1.3 Conventions

This manual uses the following conventions:

- Hexadecimal numbers are prefixed by "0x" (e.g. 0x00058C).
- *Italic* font is used for names of registers.
- **Bold** font is used for names of directories, files and OS commands.
- Palatino font is used to designate source code.
- Active low signals are followed by '#', For example, TRST#.

☞	Text in this format highlights useful or important information.

!	Text shown in this format is a warning. It describes a situation that could potentially damage your equipment. Please read each warning carefully.

The following are some of the acronyms used in this manual.

- **API** Application Program Interface
- **DAC** Digital to Analog Converter
- **LO** Local Oscillator
- **MSPS** Mega Samples per Second
- **OCXO** Oven Controlled Crystal Oscillator
- **PCI** Peripheral Component Interconnect
- **PCIe** PCI Express
- **PLL** Phase-locked Loop
- **SFDR** Spur Free Dynamic Range
- **SINAD** Signal-to-Noise and Distortion
- **SNR** Signal-to-Noise Ratio
- **TCXO** Temperature Compensated Crystal Oscillator

1.4 Manual Compatibility

The applicable hardware part numbers are defined as follows:

- Model 150-XXX(1) *Wavefront Quadrature Modulator*

(1) XXX is a three digit number that indicates the hardware variant.

1.5 Revision History

Version	Date	Description
R00	05/01/08	Initial release.
R01	11/26/08	Corrected supporting document titles

2.0 *Wavefront Quadrature Modulator* Product Family Overview

Red Rapid's *Wavefront Quadrature Modulator* product family supports direct RF modulation from your desktop. *Wavefront* is available as a standard height half-length PCI Express card complete with standard Windows™ and Linux compatible drivers. The product family includes frequency coverage and operating mode variants tailored to meet a variety of applications and budgets. A single unit is capable of supporting a frequency range from 10 MHz to 4GHz.

Key Features:

- 250 - 4000 MHz carrier synthesizer, 1MHz step size
- UHF, L-Band. S-Band, Cell Band and full band Synthesizer Variants
- Minimum +7 dBm output power across operating band
- Over 250 MHz of modulation bandwidth
- 31.5dB of output amplitude control in 0.5dB steps
- Complete software control over PCI Express bus
- Windows and Linux Drivers with sample code

The *Wavefront* family is built around a wideband quadrature modulator and broadband frequency synthesizer. The quadrature modulator features an extremely wide modulation bandwidth and operates over a very wide carrier frequency range. The on-board synthesizer features low phase noise and software controlled stepping across an extremely broad frequency range.

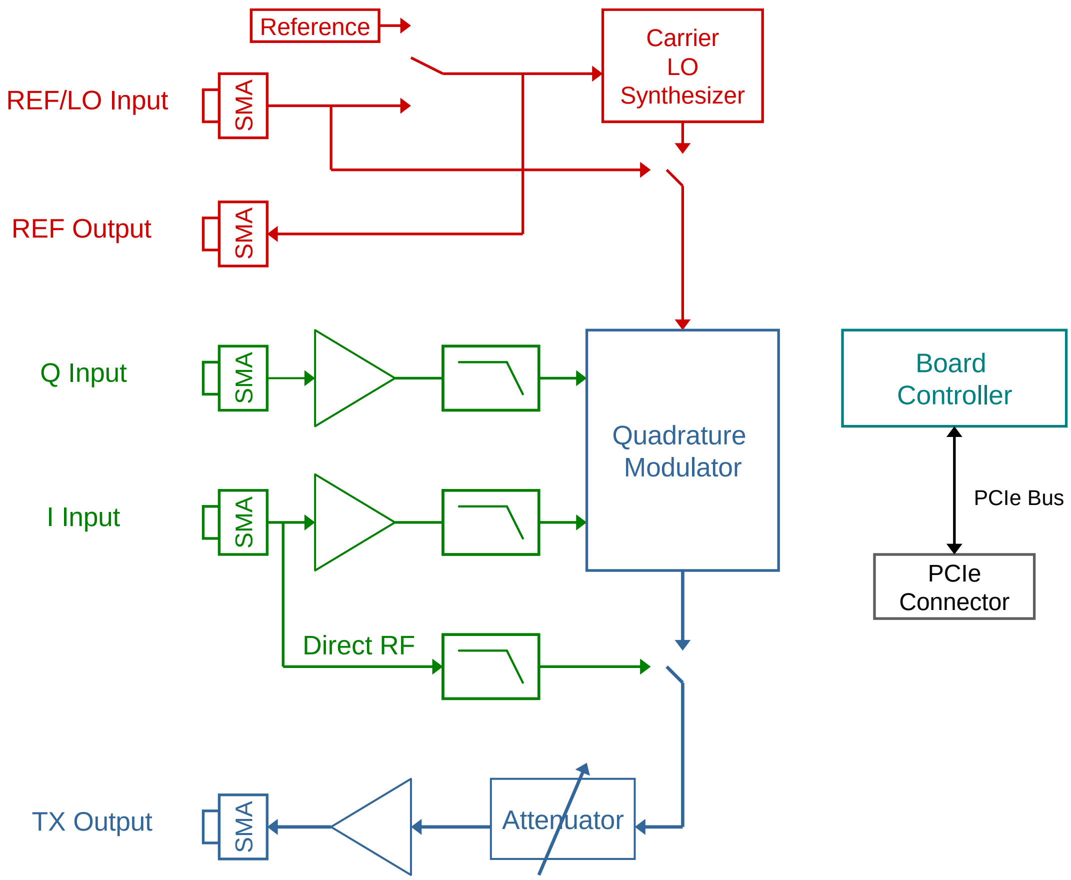


Figure 2-1 Wavefront Quadrature Modulator Block Diagram

The frequency precision of the *Wavefront* unit is controlled through the use of a reference clock. The reference clock source can be user supplied through an external interface or through the use of an on-board oven controlled crystal oscillator (OCXO) or temperature compensated crystal oscillator (TCXO).

Wavefront features an RF amplifier chain consisting of a step attenuator followed by a broadband RF amplifier. The amplifier serves to boost the modulator output to a level sufficient to operate in low power wireless environments or to drive a power amplifier in high power applications. The attenuator provides coarse level control to compensate for gain variation over frequency.

A unique feature of the *Wavefront* unit is the direct RF operating mode. The direct RF mode allows the user to bypass the quadrature modulator and directly map the I channel input to the RF output. This mode enables direct transmission of modulated signals through the same infrastructure as the quadrature modulator without changing cables.

Wavefront features ease of integration as an industry standard drop-in PCI Express card. Simple cable connections are made using SMA RF connectors. External reference presence is automatically detected and used to lock the internal synthesizer. A convenient reference clock output is available to synchronize other systems to the *Wavefront* unit.

Wavefront is controlled by a simple command set and driver that are completely compatible with Windows™ and Linux. A simple program is provided with the unit to get the user up and running right out of the box. Sample code of the program is provided to simplify user code development.

The *Wavefront* family is compatible with a number of Red Rapids' products including the FPGA-based and Instrumentation/Measurement product lines. These products feature high speed signal acquisition and generation capabilities as well as precision timing and triggering functions.

Applications:

- UMTS, GSM or CDMA Basestation
- Fixed Wireless or WLL
- ISM Transmitter
- GMSK, QPSK, QAM, SSB Transmitter
- Custom Wireless Waveforms
- Test and Measurement

3.0 Technical Specifications

3.1 Board Specifications

Table 3-1 Board Specification Summary

Specification	Value
Physical	
Form Factor	PCI Express standard height half length card
Dimensions	
Height	111.15 mm (4.376 inches)
Length	167.65 mm (6.600 inches)
Connector(1)	X4 Lane Mechanical (X1 lane electrical)
Weight	7.5 ounces
Electrical	
Board Power Supply	
+3.3V (+/- 9%)	712mA (max)
+12V (+/-8%)	622mA (max)
Power (max)	10.6W
Bus Protocol(1)	PCI Express Rev 2.0 Endpoint, single lane (X1)
Vendor ID (Hex)	0x17D2
Device ID (Hex)	0x0150
***Environmental*(2)**	
Airflow (minimum)	250 LFM
Operating Environment	
Temperature	0°C to 35°C Ambient
Humidity	90% maximum (non-condensing)
Altitude	15,000 Feet
Non-Operating Environment	
Temperature	-20°C to 65°C Ambient
Humidity	95% maximum (non-condensing)
Altitude	40,000 Feet

(1)The connector is mechanically set up for X4 link width for thermal purposes. There is only one active serial link (treat as an X1 electrically).

(2)The hardware has not been tested to the environmental specification listed in Table 3-1.

3.2 Quadrature Modulator and RF Output Specifications

Voltage and Temperature Nominal, Attenuation 0dB

Parameter	Min	Typ	Max	Unit
Operating Frequency				
Quadrature Modulator Enabled	100		4000	MHz
Synthesizer Range	250		4000	MHz
Divider Enabled	125		2000	MHz
Direct RF Mode (Modulator Bypassed)	10		150/4000	MHz
Maximum SSB Signal Output Power				
1000 MHz		+18		dBm
2000 MHz		+16		dBm
3000 MHz		+11		dBm
4000 MHz[1]		+7		dBm
P1dB				
1000 MHz		+18		dBm
2000 MHz		+17		dBm
3000 MHz		+12		dBm
4000 MHz[1]		+9		dBm
Output IP3				
1000 MHz		+30		dBm
2000 MHz		+29		dBm
3000 MHz		+24		dBm
4000 MHz[1]		+21		dBm
Noise Floor[2]				
1000 MHz		-140		dBm/Hz
2000 MHz		-140		dBm/Hz
3000 MHz		-140		dBm/Hz
4000 MHz[1]		-134		dBm/Hz
Carrier Suppression[3]				
Uncalibrated		-20		dBc
Calibrated (100 MHz Span)		<-60		dBc
Calibrated (Full Operating Range)		<-40		dBc
Sideband Suppression[4]				
Uncalibrated		-20		dBc
Calibrated (+/-1MHz span)		<-60		dBc
Calibrated (+/-5MHz span)		<-40		dBc
Output Impedance		50		Ohms
Attenuator				
Range	0		31.5	dB
Step size		0.5		dB
Output Lowpass Filter				
3dB Cutoff		5580		MHz
20dB Cutoff		6850		MHz

Notes: [1]Values for 4 GHz are estimates
[2]Noise floor estimated for 20MHz offset from carrier
[3]Carrier suppression calibrated for a single carrier frequency and measured across frequency span

[4]Sideband suppression calibrated for a single carrier offset and measured across offset span. Sideband suppression performed by adjusting phase offset between I and Q legs off board (no phase offset adjustment id available on Model 150).

3.3 Baseband Input Specifications

Parameter	Min	Typ	Max	Unit
Input Impedance		50		Ohms
Input Coupling		DC		
Full Power Input Level				
Voltage (50 Ohms)		0.71		Vpp
Power (50 Ohms)		+1		dBm
Input Bandwidth(3 dB) [(1)]				
Unfiltered		700		MHz
Standard Filter		45		MHz
Input DC Level Range	-0.1	0	+0.1	V
DC Offset Adjustment				
Range	-150		+150	mV
Resolution		146		uV/CNT

[(1)] Input bandwidth is set by on-board filter limits.

3.4 Direct RF Mode Specifications

Parameter	Min	Typ	Max	Unit
Input Impedance		50		Ohms
Input Coupling		AC		
RF Chain Parameters				
Gain (0dB atten)		10.5		dB
Noise Figure		12		dB
Input IP3		+23		dBm
Output Compression		+19		dBm
Attenuator				
Range		31.5		dB
Resolution		0.5		dB/step
Frequency Response [(1)]				
1dB Limits	10		130	MHz
3dB Limits	5		148	MHz
50dB Limits	1		194	MHz
Rejection Level		65		dB
LO Leakage [(2)]		-65		dBm

[(1)] Bandwidth set by on-board filter limits.

[(2)] Unmodulated LO leak level through common switch

3.5 Internal/External Carrier LO Specifications

Parameter	Min	Typ	Max	Unit
Internal Carrier Synthesizer				
Frequency Range	250		4000	MHz
Frequency Step Size		1		MHz
Settle Time (to within 1kHz)		3		ms
Phase Noise				
10kHz Offset		-80		dBc/Hz
100kHz Offset		-110		dBc/Hz
Harmonics			-15	dBc
Spurious			-50	dBC
External Carrier LO Input (AC Coupled)				
Input Impedance		50		Ohms
Frequency Range	100		4000	MHz
Input Level (100 – <3500MHz)	-3.5	+2.5	+8.5	dBm
Input Level (>3500-4000MHz)	+2.5	+2.5	+8.5	dBm

3.6 Internal/External Reference Specifications

Parameter	Min	Typ	Max	Unit
Internal Reference (TCXO)				
Frequency		10		MHz
Frequency Stability	-1.5		+1.5	ppm
Phase Noise (100 Hz Offset)			-113	dBc/Hz
Phase Noise (10 kHz Offset)			-150	dBc/Hz
Internal Reference (OCXO)				
Frequency		10		MHz
Frequency Stability	-10		+10	ppb
Phase Noise (100Hz Offset)			-140	dBc/Hz
Phase Noise (10 kHz Offset)			-150	dBc/Hz
External Reference Input (AC-Coupled)				
Impedance		50		Ohms
Frequency	10		10	MHz
Power Level (50 Ohms)	+7		+14.8	dBm
Maximum harmonic levels				
40 MHz			+2	dBm
50 MHz			-2	dBm
>60MHz			-15	dBm
External Reference Output (AC-Coupled)				
Impedance		50		Ohms
Power Level		+7		dBm

4.0 Absolute Maximum Specifications

Stresses above those listed in Table 4-1 may cause damage to the unit. The operation of the unit at these or any other conditions outside of those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect unit reliability.

Table 4-1 Absolute Maximum Specifications

Parameter	Min	Typ	Max	Unit
Environmental (Inlet Air)				
Operating Temperature	-30		50	C
Operating Airflow	250			LFM
Non-Operating Temperature	-30		85	C
Baseband Inputs (50 Ohms)				
DC Level + AC Peak	-1.3		3.3	V
AC Voltage Swing			1.125	Vpp
AC Input Power			5	dBm
Transmitter Output				
Reverse DC Voltage	-10		+10	V
Reference Input (50 Ohms)				
DC Level	-10		10	V
AC Swing			4.5	Vpp
AC Power			+17.5	dBm
External Carrier LO Input (50 Ohms)				
DC Level	-10		10	V
AC Swing			2.5	Vpp
AC Power			+12	dBm

!	Exposure to absolute maximum conditions for extended periods may degrade unit reliability.

5.0 Characterization Plots

5.1 Baseband Input Standard Filter Response

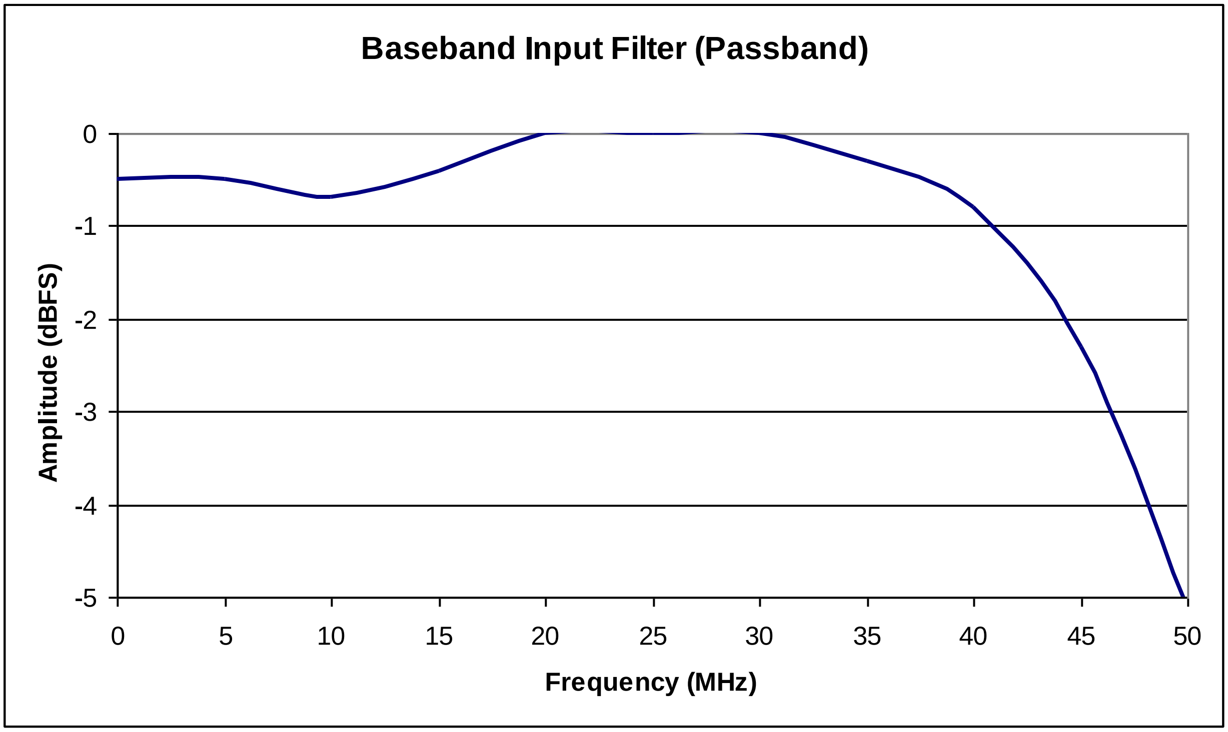


Figure 5-1 Baseband Input Filter Passband Response

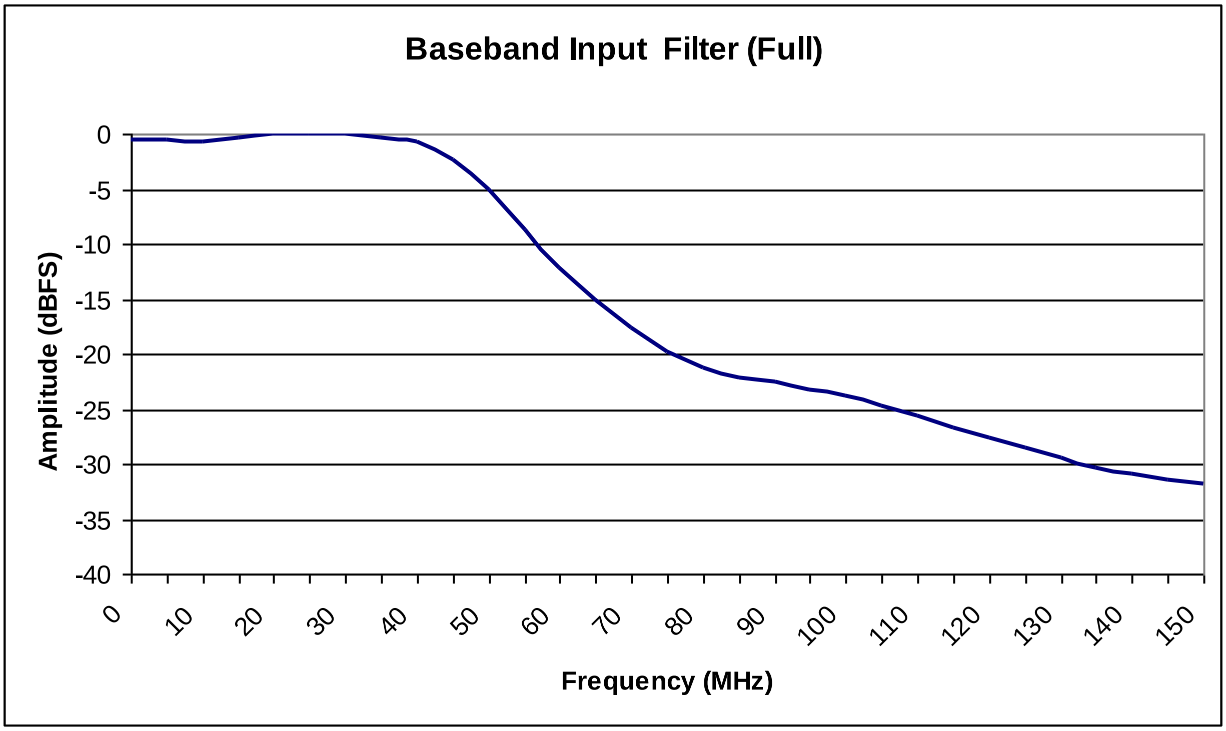


Figure 5-2 Baseband Input Filter Full Response

5.2 Direct RF Mode Standard Filter Response

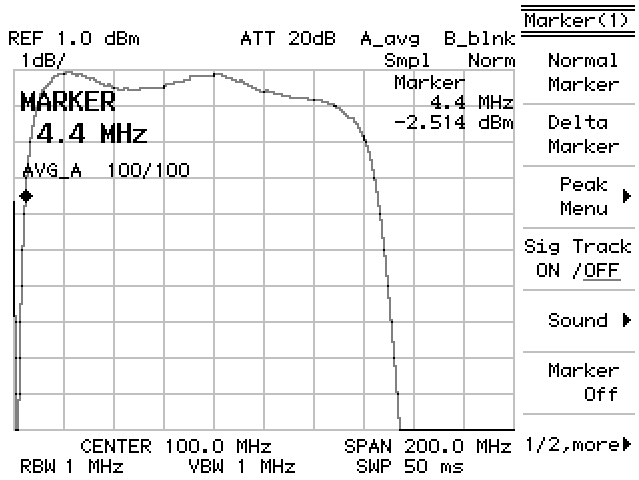


Figure 5-3 Direct RF Mode Filter 200MHz Span 1dB Per Div

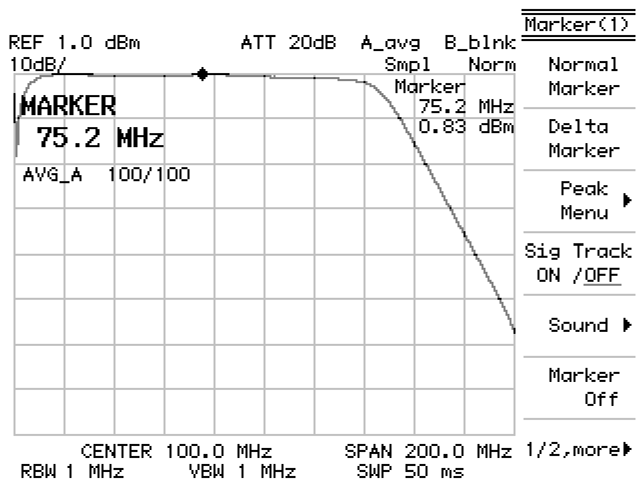


Figure 5-4 Direct RF Mode Filter 200MHz Span 10dB Per Div

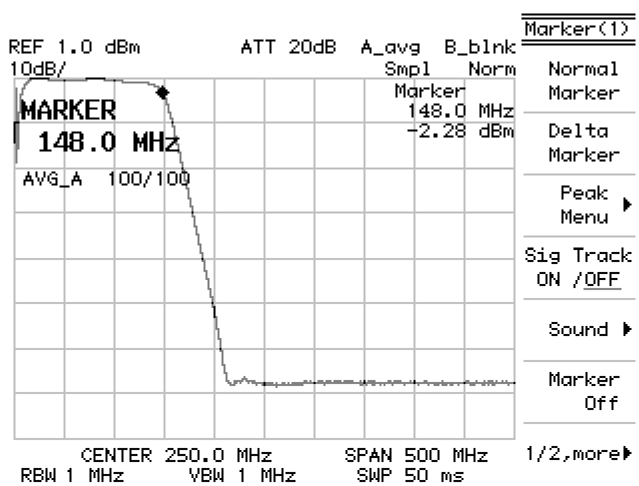


Figure 5-5 Direct RF Mode Filter 500MHz Span 10dB Per Div

5.3 Output Power vs Frequency

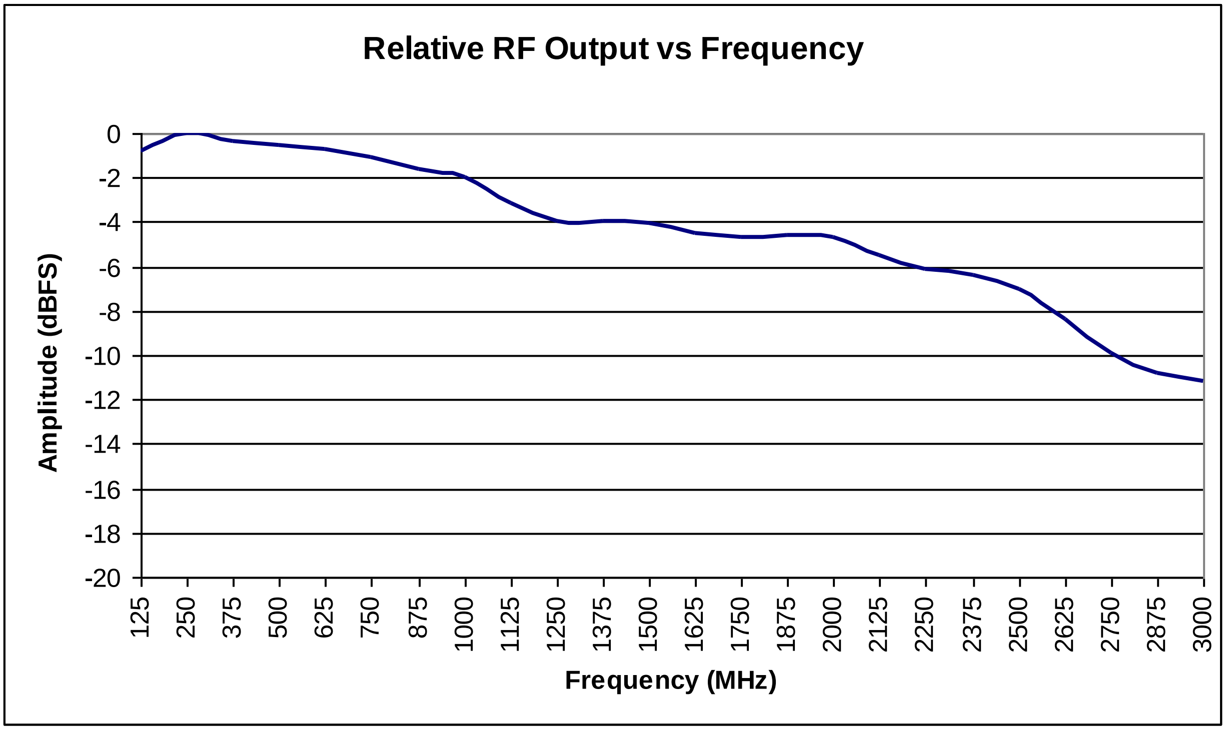


Figure 5-6 Relative RF Output vs Frequency

5.4 Relative Carrier Harmonic Content

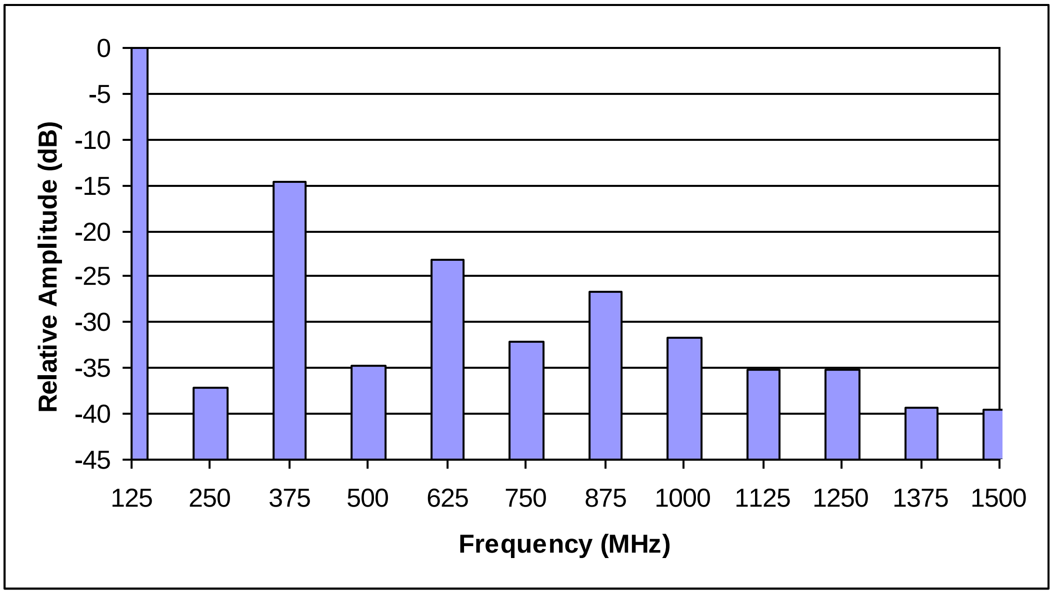


Figure 5-7 Harmonic Content for 125MHz Tone (DIV Mode)

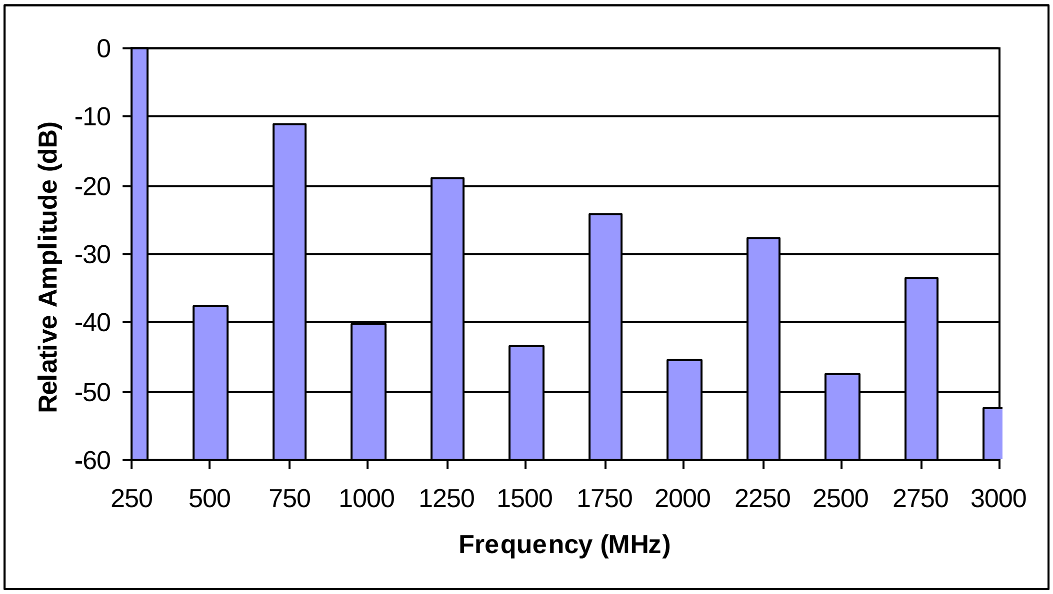


Figure 5-8 Harmonic Content for 250MHz Tone

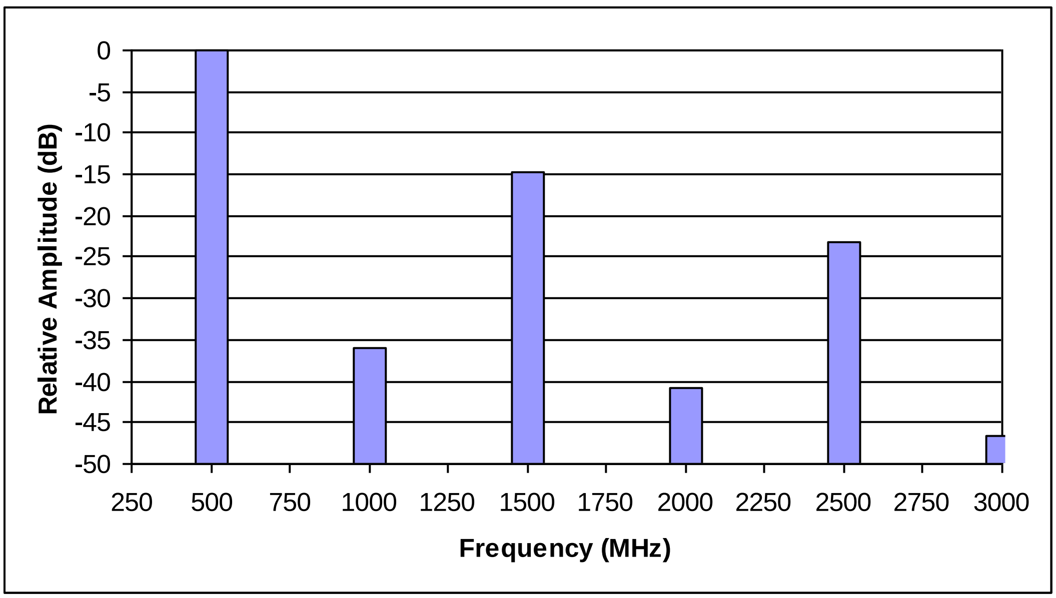


Figure 5-9 Harmonic Content for 500MHz Tone

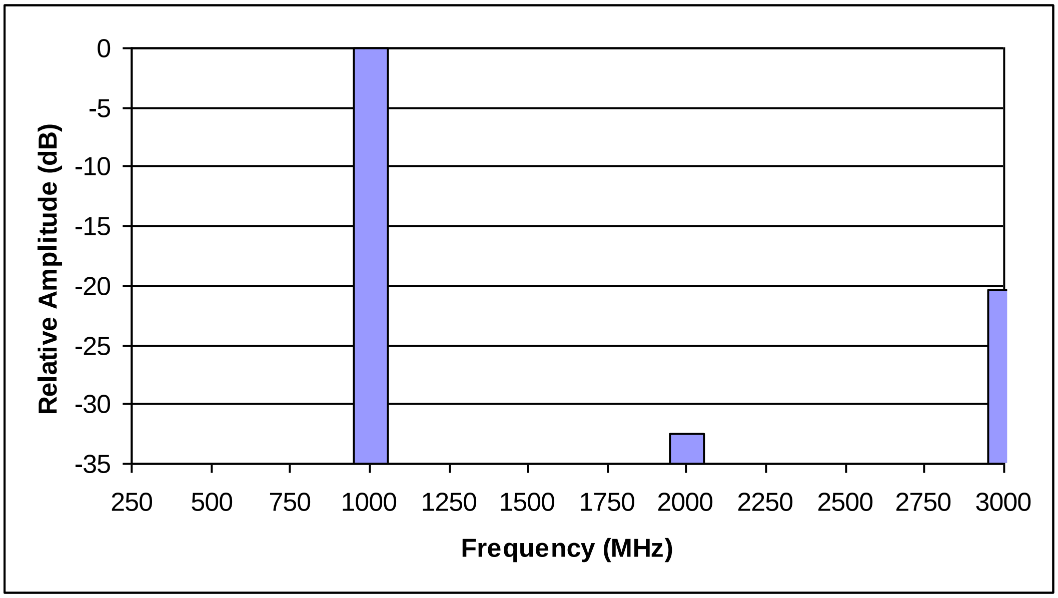


Figure 5-10 Harmonic Content for 1000MHz Tone

5.5 Carrier Suppression vs Frequency

The plot shown in Figure 5-11 illustrates unit carrier suppression performance over the operating frequency range with carrier suppression optimized for a single point at 1000 MHz.

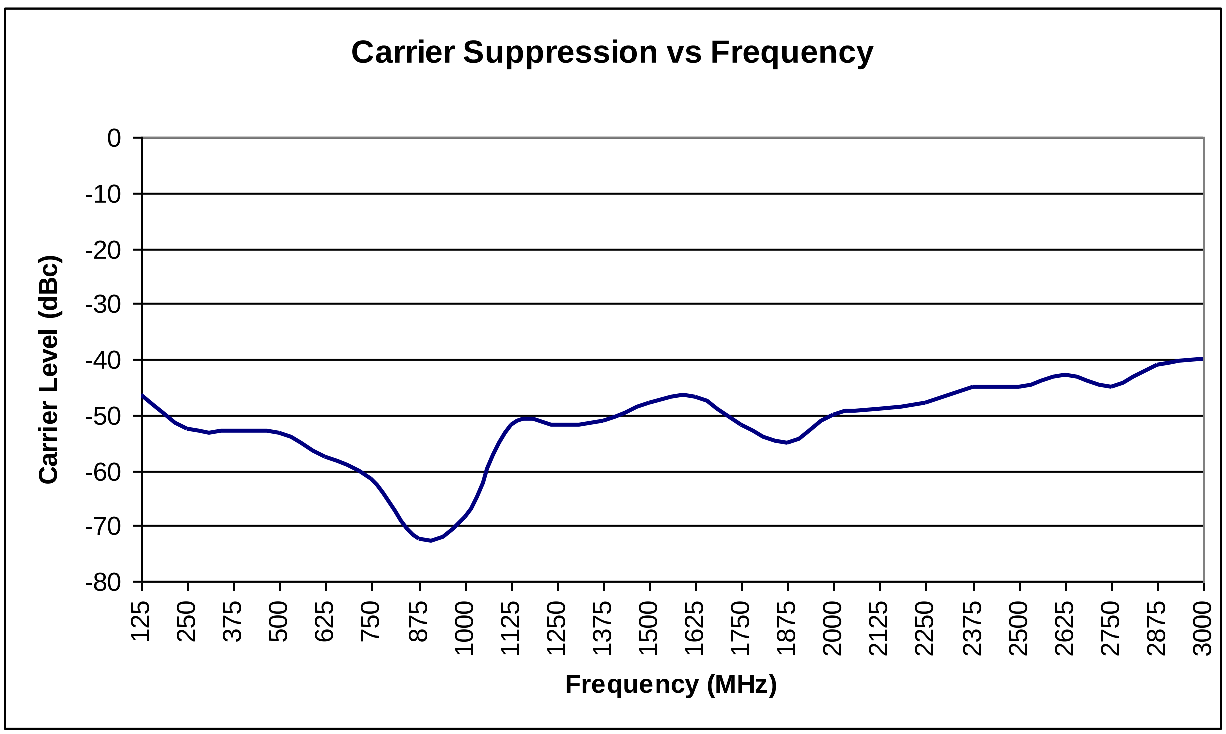


Figure 5-11 Carrier Suppression vs Frequency (Optimized for 1000 MHz)

The plot shown in Figure 5-12 illustrates unit carrier suppression performance over the operating frequency range with carrier suppression optimized for 1500 MHz.

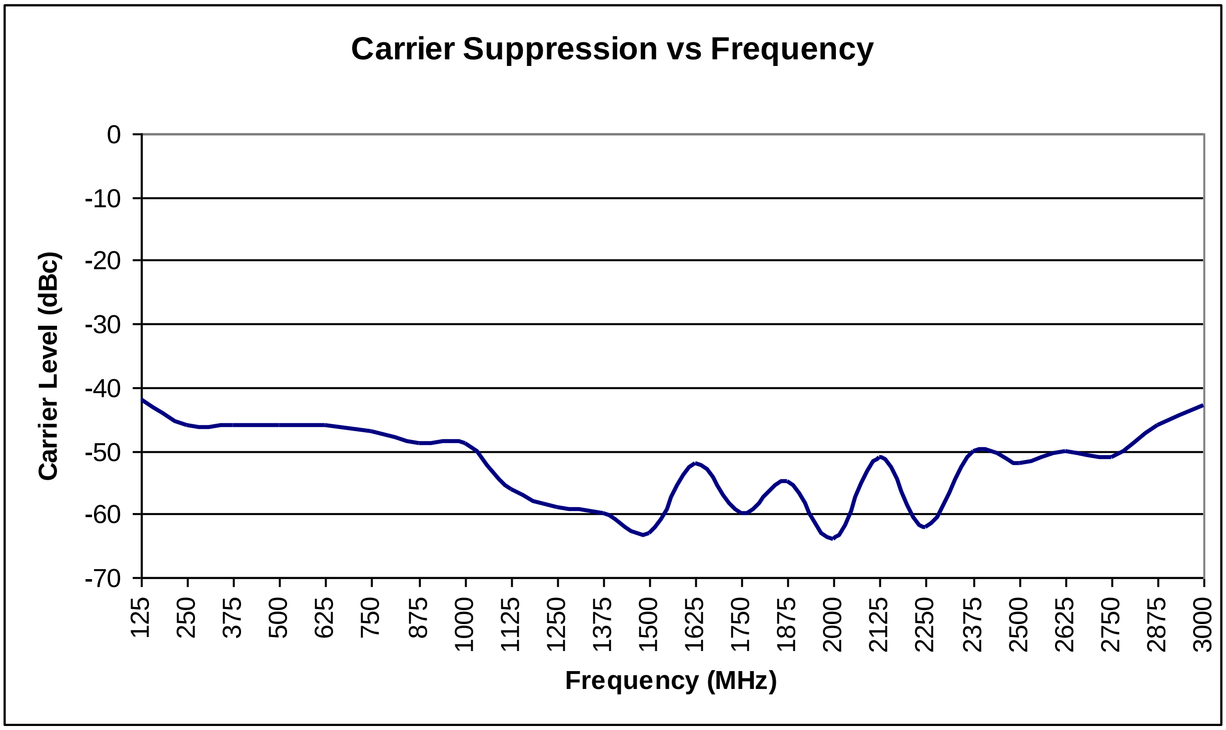


Figure 5-12 Carrier Suppression vs Frequency (Optimized for 1500 MHz)

5.6 Sideband Suppression vs Carrier Offset Frequency

The following plots examine sideband suppression performance versus carrier offset frequency when optimized for operation at a single offset point. All plots measured with a carrier frequency of 1000 MHz.

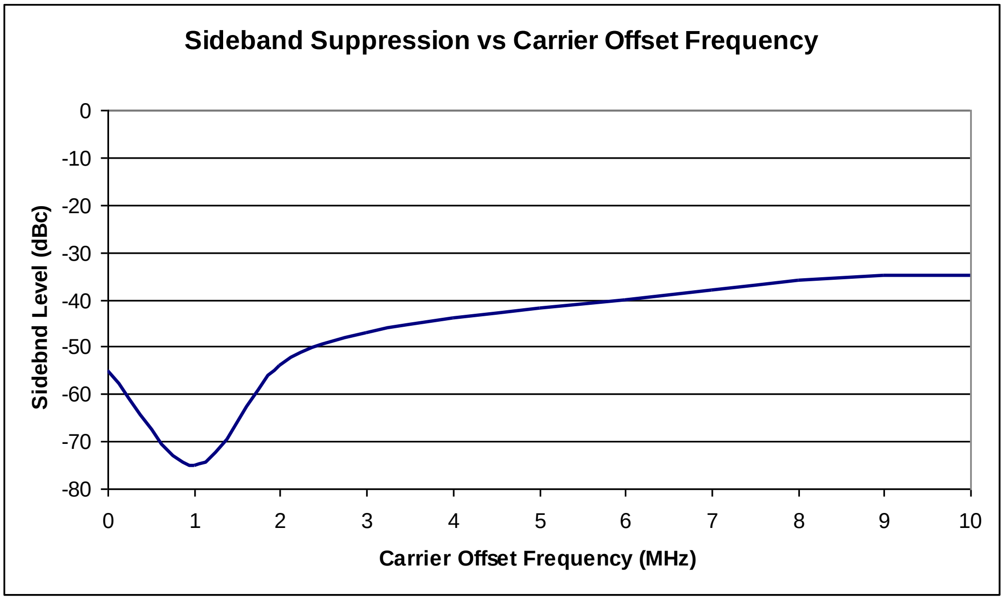


Figure 5-13 Sideband Suppression vs Carrier Offset Frequency (Optimized for 1 MHz Offset)

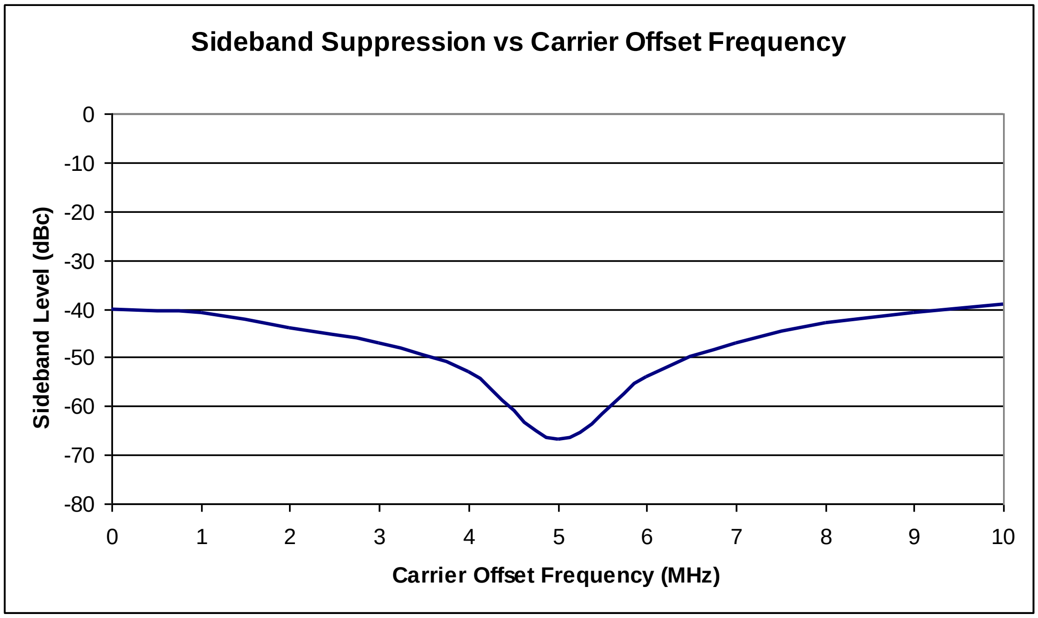
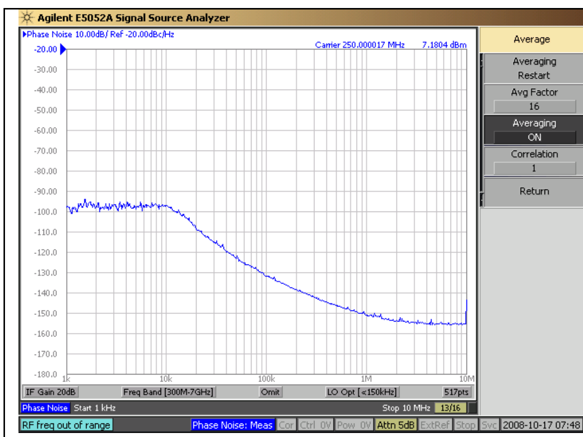
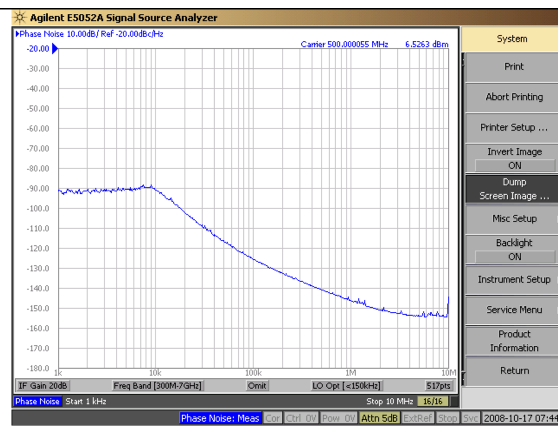


Figure 5-14 Sideband Suppression vs Carrier Offset Frequency (Optimized for 5 MHz Offset)

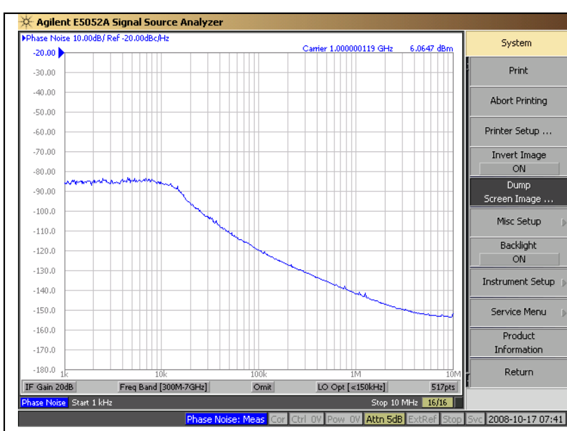
5.7 Synthesizer Phase Noise Plots



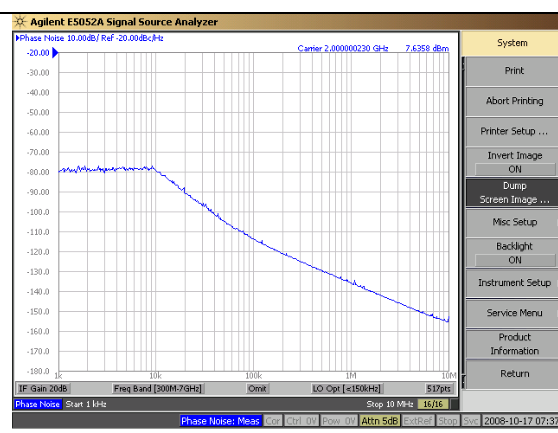
Phase Noise at 250 MHz



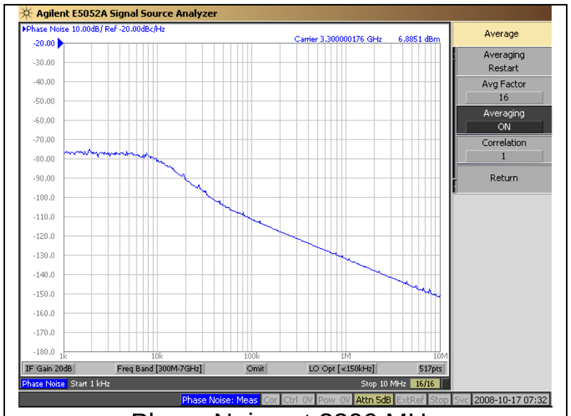
Phase Noise at 500 MHz



Phase Noise at 1000 MHz



Phase Noise at 2000 MHz



Phase Noise at 3300 MHz

5.8 Application Spectrum Plots

The following application plots were made using an Agilent N5182A MXG RF Vector Signal Generator as a baseband input source for the Model 150. The output put of the Model 150 was analyzed using an Agilent 9020A MXA Signal Analyzer for a number of standard waveforms.

5.8.1 CDMA 2K Waveform at 1 GHz

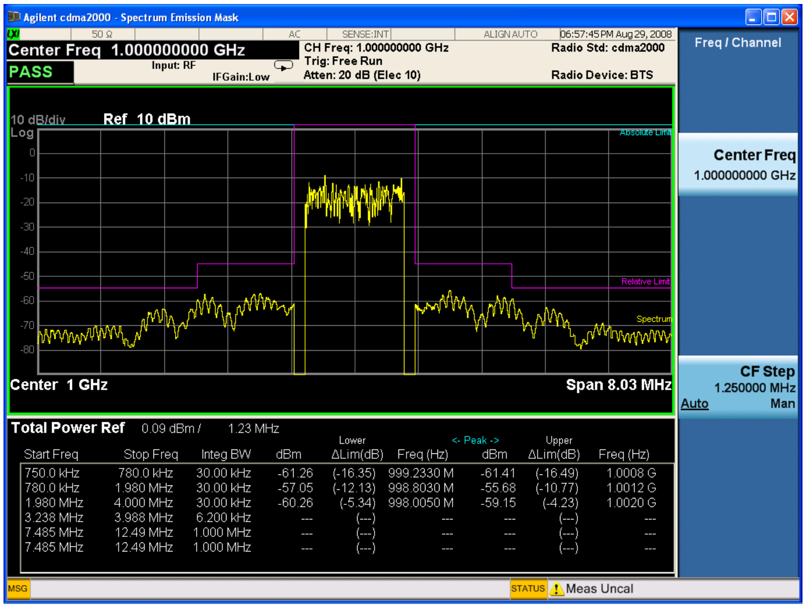


Figure 5-15 CDMA 2K Spectrum Emission Mask

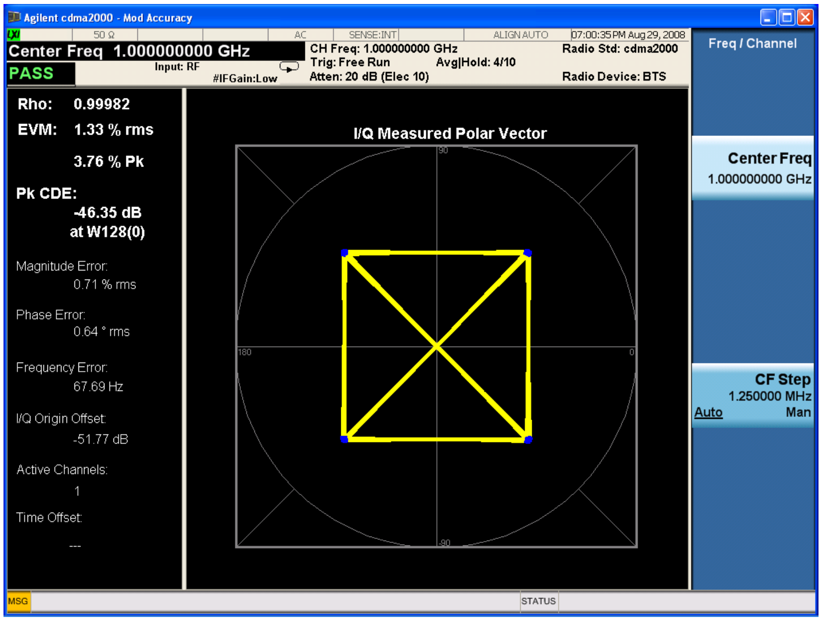


Figure 5-16 CDMA 2K Modulation Accuracy

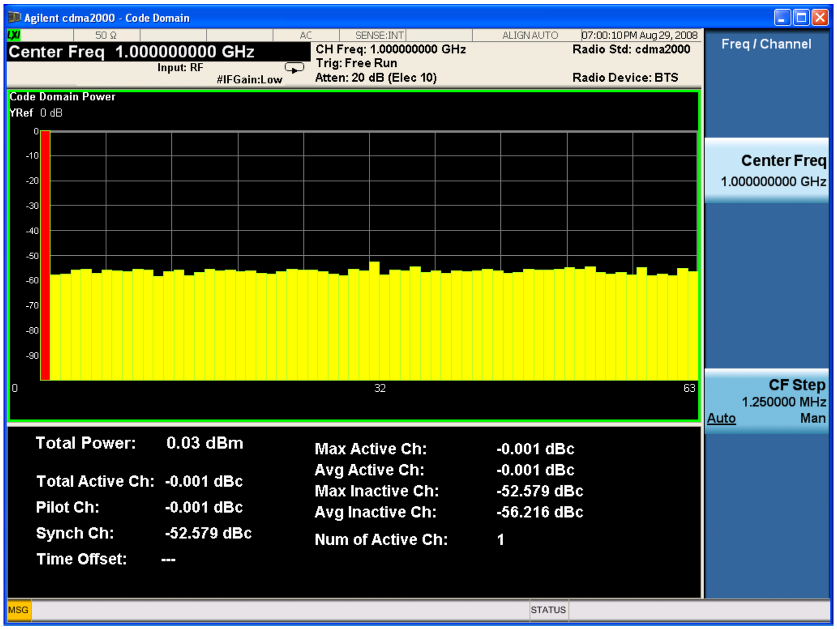


Figure 5-17 CDMA 2K Code Domain

5.8.2 QPSK Waveform at 1 GHz

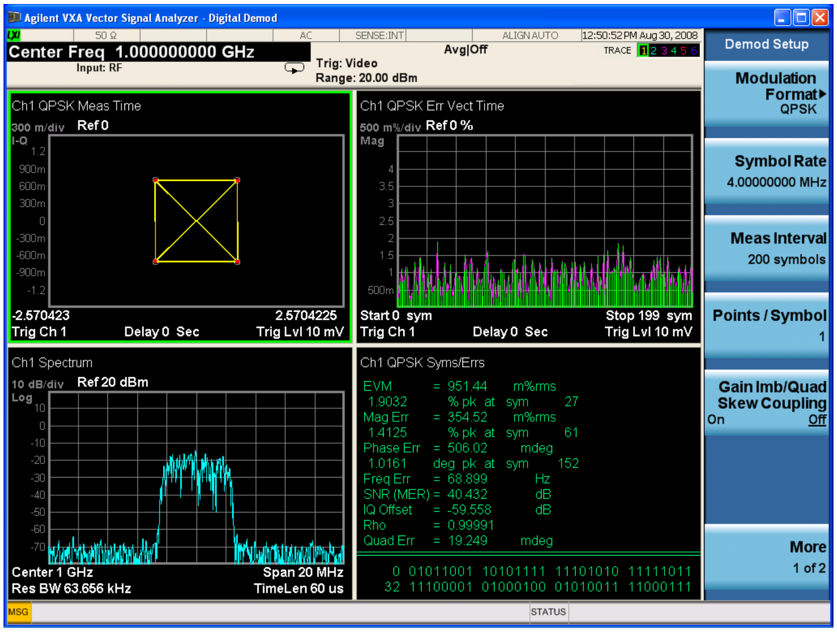


Figure 5-18 QPSK Waveform (4 Msymbols)

5.8.3 QAM16 Waveform at 1 GHz

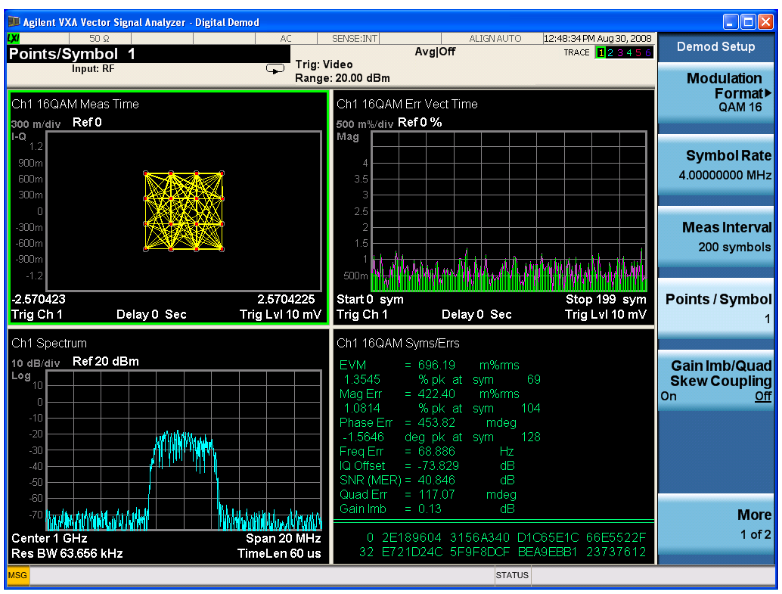


Figure 5-19 QAM16 Waveform (4 Msymbols)

6.0 Hardware Description

A block diagram of the Model 150 Quadrature Modulator hardware is shown in Figure 6-1. The hardware is made up of four major functional blocks: baseband inputs, carrier LO generation, quadrature modulator/RF output chain and board controller. The primary use of the Model 150 is as a quadrature modulator where users apply analog data to the baseband inputs to modulate a carrier LO. A secondary mode of operation allows the user to bypass the quadrature modulator and transmit the I baseband input directly out the TX port. This secondary mode of operation, called direct RF mode, provides support for the transmission of user generated RF waveforms. The primary purpose for the direct RF mode is to provide frequency coverage below the lower operating frequency limit of the on-board modulator.

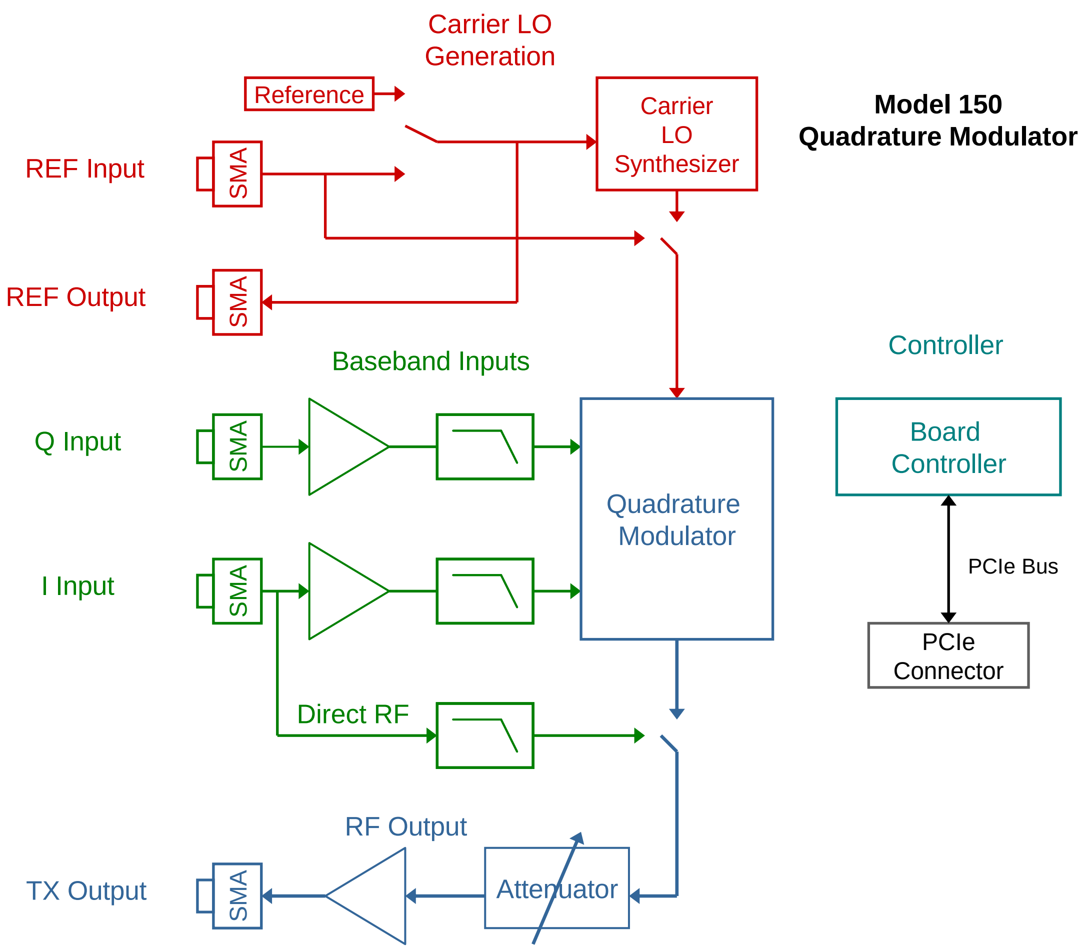


Figure 6-1 Model 150 Block Diagram

There are two analog inputs to the quadrature modulator labeled I and Q. Each dc-coupled input is amplified, offset adjusted and applied to the quadrature modulator input. The broadband inputs feature a software controlled offset adjustment for improving carrier rejection.

The Model 150 modulator receives its carrier from one of two sources; an on-board synthesizer or a user supplied external carrier. The user also has the choice of supplying their own reference source or using one of the built-in references for the on-board synthesizer.

The modulator board features a broadband RF section consisting of a digitally controlled step attenuator followed by a wideband amplifier. The attenuator provides coarse level control while the amplifier boosts the modulator output across the operating band.

The Model 150 is an industry standard PCI express card that supports the Windows and Linux operating systems. Control of the 150 is handled by simple software commands interpreted by a central board controller. The board controller converts software commands issued over the express bus into to discrete control signals to various board functions.

The following paragraphs describe the hardware functions of the Model 150 in detail.

6.1 Baseband Inputs

Analog data is presented to the quadrature modulator via the Wavefront baseband inputs. Each baseband coaxial input is DC-coupled, amplified and passed through a lowpass filter prior to being applied to the quadrature modulator inputs as shown in Figure 6-2. Each input can be DC level adjusted under user software control to reduce carrier feedthrough.

The "I" input leg can be used in what is referred to as "Direct RF" mode. In this mode the I input bypasses the modulator and is routed through a filter, attenuator, amplifier chain and out the RF port. The following paragraphs describe the workings of the DC level offset adjustment, filtering and direct RF functions.

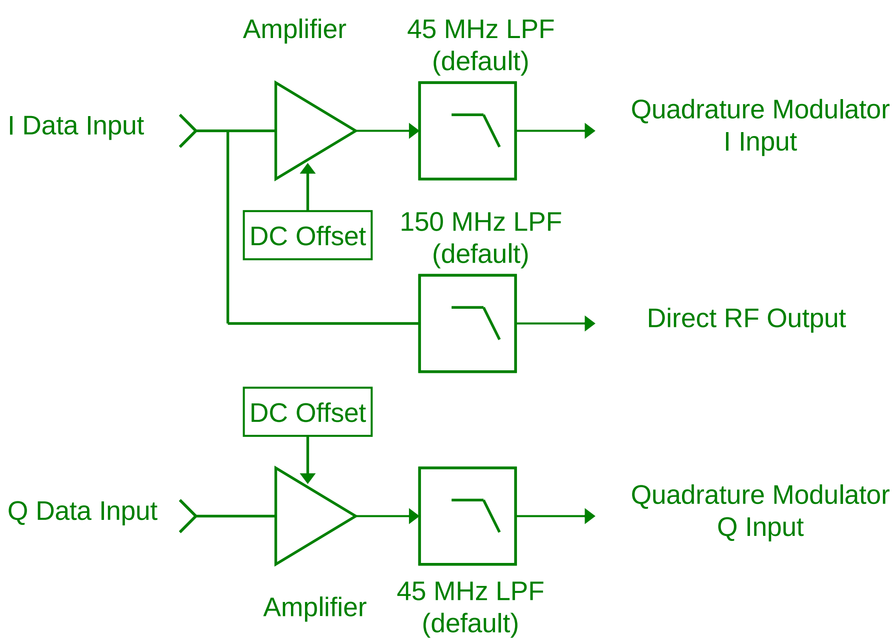


Figure 6-2 Baseband Inputs

6.1.1 DC Offset Adjustment (Carrier Suppression)

The I and Q baseband inputs can be independently adjusted for DC offset under user software control. The DC offset control can be used to balance the DC level between the I and Q inputs to reduce the amount of carrier feed through seen at the quadrature modulator output. The DC adjustment for each input consists of two DACs arranged in a "push-pull" configuration for each baseband input. A diagram of the I input offset structure is shown in Figure 6-3. The Q baseband input structure is identical. One DAC pushes the offset in a positive direction while the other pulls the offset in a negative direction. Only one offset DAC of the push-pull pair should be active (nonzero) at any given time to prevent driving the input out of the amplifier common mode range. Note each baseband input can be offset independently. For more information on user control see the *Wavefront Software Manual*.

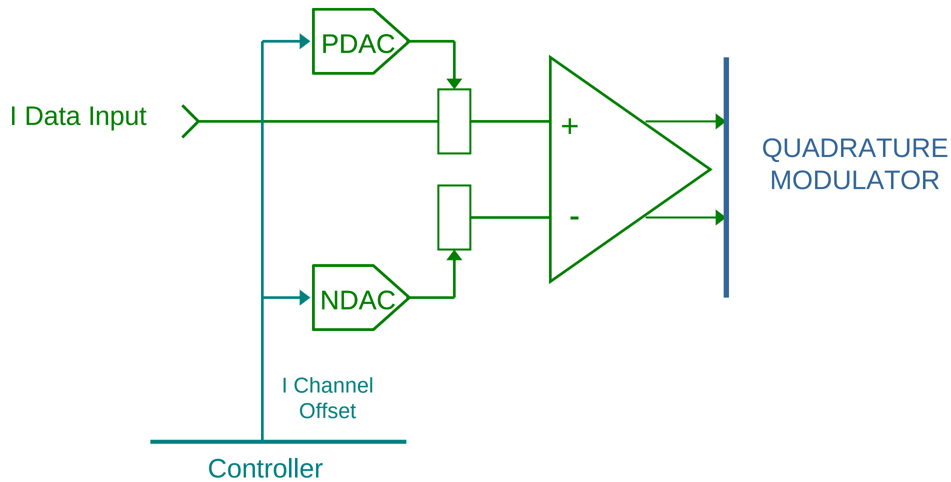


Figure 6-3 I Channel Input DC Offset Diagram

☞	Only one of the pair of offset DACs per input should be active at one time.

6.1.2   *Phase Adjustment (Sideband Suppression)*

Undesired sideband suppression is accomplished by balancing the phase offset and amplitude gain between the I and Q legs of the quadrature modulator. The Model 150 has no mechanism for balancing gain or phase of the baseband inputs. All phase and gain adjustments must be applied to the baseband inputs off board. The calibrated sideband suppression performance data used in this manual were generated using a Red Rapids Model 332 that has built-In phase offset and gain balance adjustments.

☞	The Model 150 has no built-in phase and gain balance adjustment capability for the baseband inputs.

6.1.3   *Input Filtering*

The Model 150 provides lowpass filters on the baseband inputs to condition signals as shown in Figure 6-4. The default filter for the baseband inputs is a 45 MHz Chebyshev. The filter is used to limit amplifier noise and distortion and may be used to remove input images. Plots of the standard filter response are presented in section 5.1. Other filter types and cutoffs are available as a build option see section 8.0 for more details.

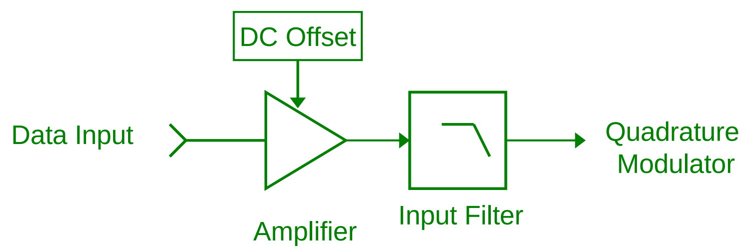


Figure 6-4 Baseband Input Filter Location

6.1.4 Direct RF Output

The I channel baseband input can be routed directly to the RF output via user software command. This feature allows the user to bypass the quadrature modulator and directly transmit a waveform through the RF channel as shown in Figure 6-5. Ostensibly the direct RF mode provides support for modulated signal transmission below the quadrature modulator lower frequency limit. The direct RF mode serves as a vehicle to share the RF port output over an extended frequency range.

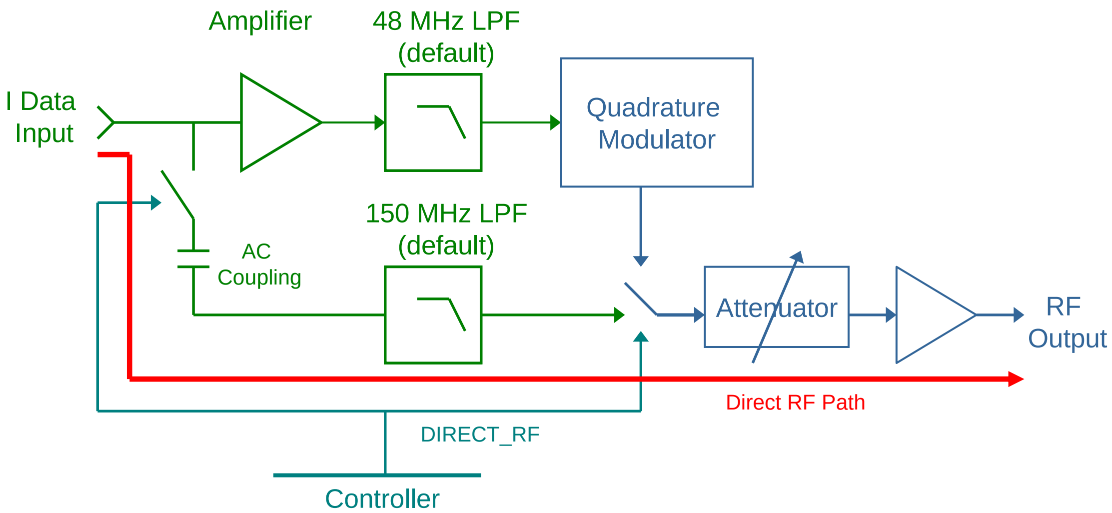


Figure 6-5 Direct RF Output Diagram

The direct RF mode path contains an independent lowpass filter tailored for direct RF signal content. The default filter design is a 150 MHz, 7^{th} order elliptic filter of type C07 20 theta = 44 plots of which are shown in section 5.2. The filter type and cutoff frequency for the direct RF mode path may be changed as a build option. See section 8.0 for more information on build options.

6.2 Carrier LO Generation

The carrier local oscillator is a sinewave that is modulated by the baseband inputs inside the quadrature modulator unit and transmitted as a modulated carrier. A block diagram of the carrier LO generation structure is shown in Figure 6-6. The carrier LO can be sourced from the internal synthesizer or an external source applied to the reference input SMA connector.

The Model 150 features an on-board broadband synthesizer that can be phase locked to an internal TCXO or an external reference applied to the reference input SMA. The internal synthesizer can be divided by two to generate carrier frequencies a sub-octave below the on-board synthesizer’s lower frequency limit. A copy of the synthesizer reference clock is available from the reference output SMA. The following paragraphs describe the carrier LO carrier control and generation functions in detail.

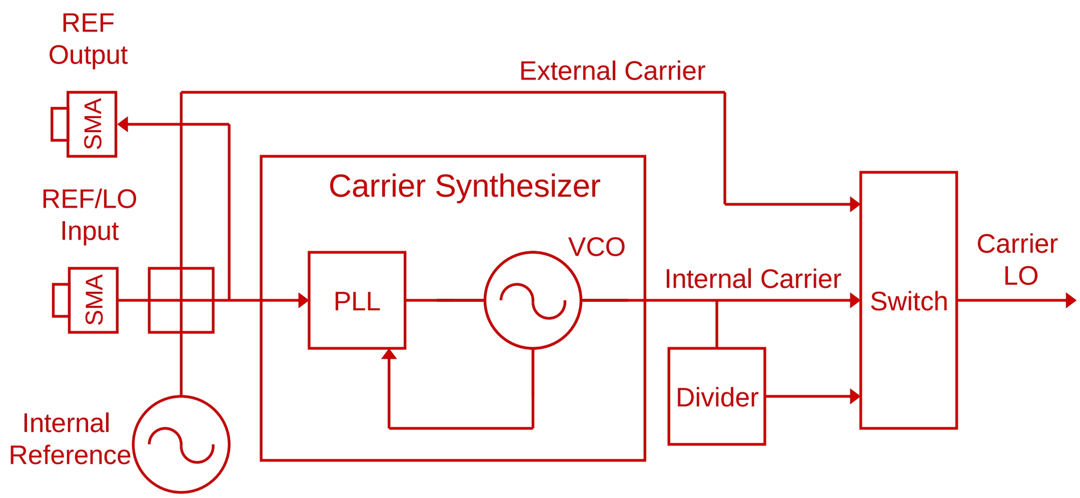


Figure 6-6 Carrier LO Control and Generation

6.2.1 Carrier Synthesizer (Internal Carrier)

The carrier synthesizer is a phase-locked loop sinewave source that operates across a broad frequency range. The synthesizer provides the RF carrier or local oscillator for the quadrature modulator. A block diagram of the carrier synthesizer is shown in Figure 6-7. The Synthesizer is locked to a reference clock for stability and is tuned across the operating frequency band in discrete steps. The unit is tuned via user commands issued to the board controller over the PCI express bus.

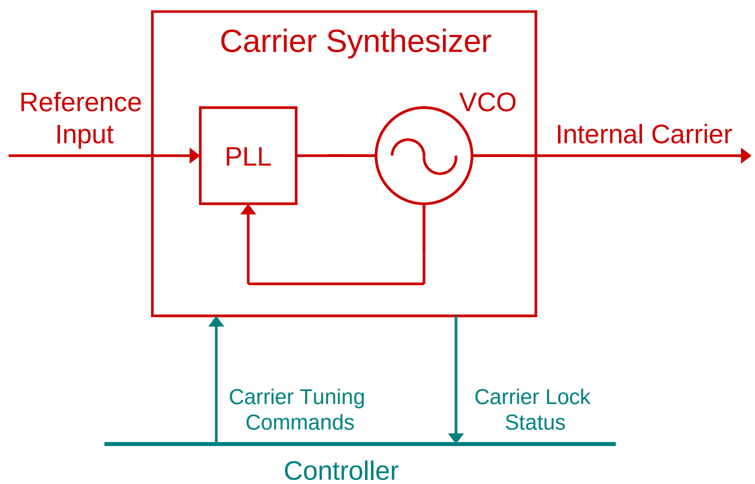


Figure 6-7 Carrier Synthesizer

A detailed block diagram of the PLL synthesizer structure is shown in Figure 6-8. The diagram shows how the R and N counter registers are used to tune the synthesizer frequency. The synthesizer is tuned in discrete steps as determined by the divided down reference clock value. The synthesizer has a fixed step size of 1MHz; therefore the R counter is always set to 10 (10 MHz/10 = 1MHz). The divided reference clock is fed to a phase comparator. The phase comparator compares the phase of the divided reference clock to that of the divided clock from a voltage controlled oscillator VCO. The comparator advances or retards the VCO using a tuning voltage until the phase of the divided VCO matches the phase of the divided reference. The clock output characteristics track those of the reference clock. The equation governing the final output frequency is:

*Output Frequency = (Reference Frequency/R Counter Value) * N Counter Value*

Substituting the known values for the Model 150 yields:

*Output Frequency (MHz) = 1 (MHz) * N Counter Value*

Or

N Counter Value = Output Frequency (MHz)

Once the R counter is initialized, the user simply tunes the Carrier Synthesizer by writing the desired tuning frequency value to the N counter register.

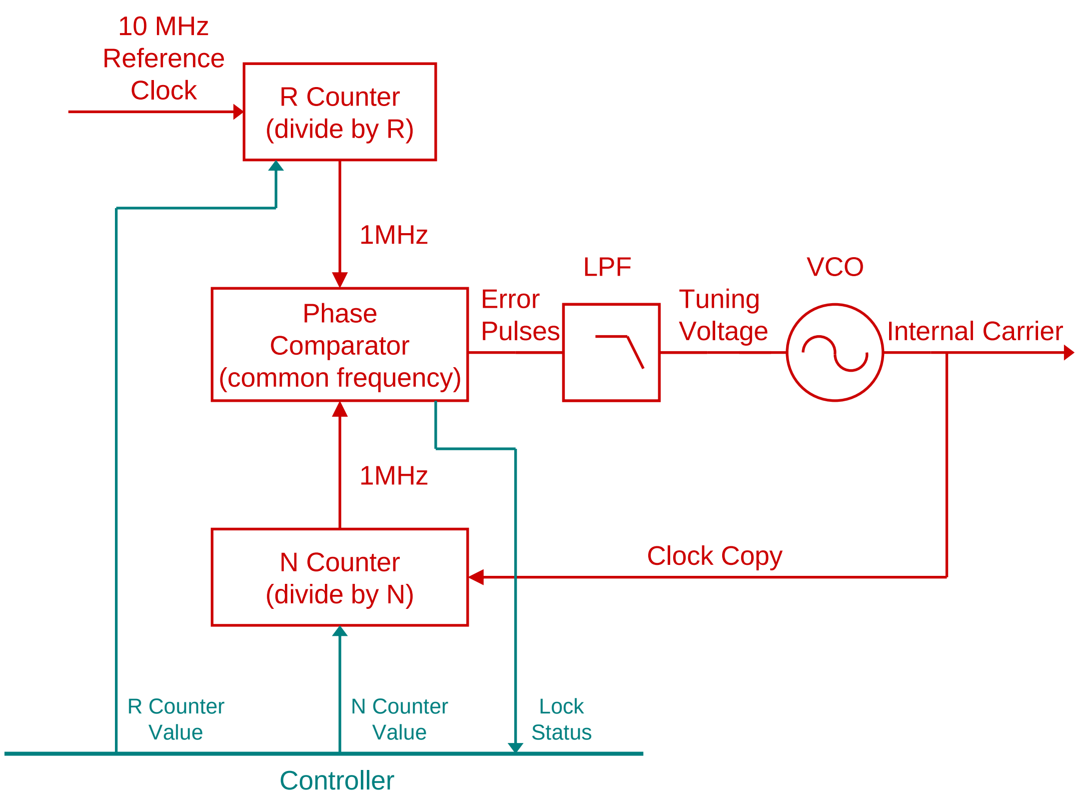


Figure 6-8 PLL synthesizer block diagram

☞	The R counter value should always be set to 10, the N counter value is the desired output frequency in MHz.

PLL synthesizers are closed loop control structures and require a period of time to “lock” to a commanded frequency. This locking period is referred to as settle time and is defined as the time required to pull the synthesizer within a window of the commanded frequency. Generally settle time is proportional to the separation in commanded versus current frequency. The synthesizer provides a lock indication to the user through the board controller.

☞	The synthesizer lock status should be ignored when using an external LO.

6.2.2 Internal Carrier Divider

An internal carrier divider is provided to extend the carrier LO range down one suboctave. The internal carrier synthesizer has a lower limit of 250 MHz. The divider extends operation of the on-board modulator down to a carrier frequency of 125 MHz. The divide-by-two circuit can be enabled under user command to cover the carrier range between 125 MHz and 250 MHz as shown in Figure 6-9. The divider can operate at higher operating frequencies if desired.

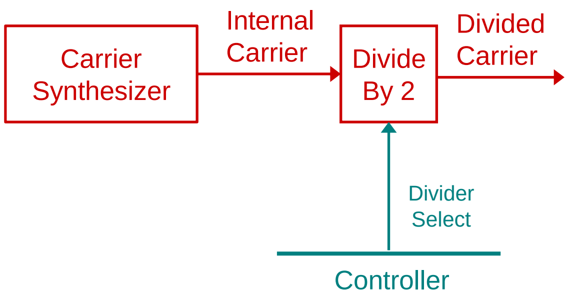


Figure 6-9 Carrier Divider Diagram

The divided carrier output is steered by commanding the carrier synthesizer to twice the desired frequency and enabling the output divider. The divider is not connected to the external carrier input. The effective step size of the carrier LO with the divider enabled is 500 kHz.

☞	Set the internal carrier synthesizer to twice the desired frequency when using the divider.

6.2.3 Reference Clock

The Model 150 features a number of reference options to match stability requirements and cost. The user has the choice of using one of two built-in reference options or supplying their own external reference clock. Red Rapids offers the choice of a TCXO or a more expensive and accurate OCXO as a build option. Applications requiring synchronization to a master frequency reference can use the external reference input. The reference input is amplified and made available to the reference output port to support reference clock distribution.

The Model 150 has an internal TCXO or OCXO for use as the default reference clock for the carrier synthesizer. The synthesizer can be phase locked to an external 10 MHz system reference to achieve system-wide phase coherence by simply connecting a source to the reference input SMA connector as shown in Figure 6-10. The AC power level on the reference input is continuously monitored to automatically detect the presence of an external source. If the power level exceeds the established threshold, the external reference source is switched in to the carrier synthesizer. Hysteresis is built into the detection circuit to prevent oscillation around the threshold. The status of the reference clock detector is passed to the user via the on-board controller. Only a high quality low phase noise (< -145dBc/Hz @ 10 kHz) source should be used as an external reference. The harmonic content of any user supplied reference clock should be limited to prevent the reference from being mistaken for an external carrier source. The harmonic content limit is listed in section 3.6.

A copy of the reference clock is amplified and routed to the front panel reference output connector for use in reference clock distribution. Power to the reference output clock buffer amplifier is under software control. Power to the amplifier can be disabled to reduce radiated emissions. Reference level specifications can be found in section 3.0.

☞	The harmonic content of any user supplied reference clock should be limited as specified in section 3.6.

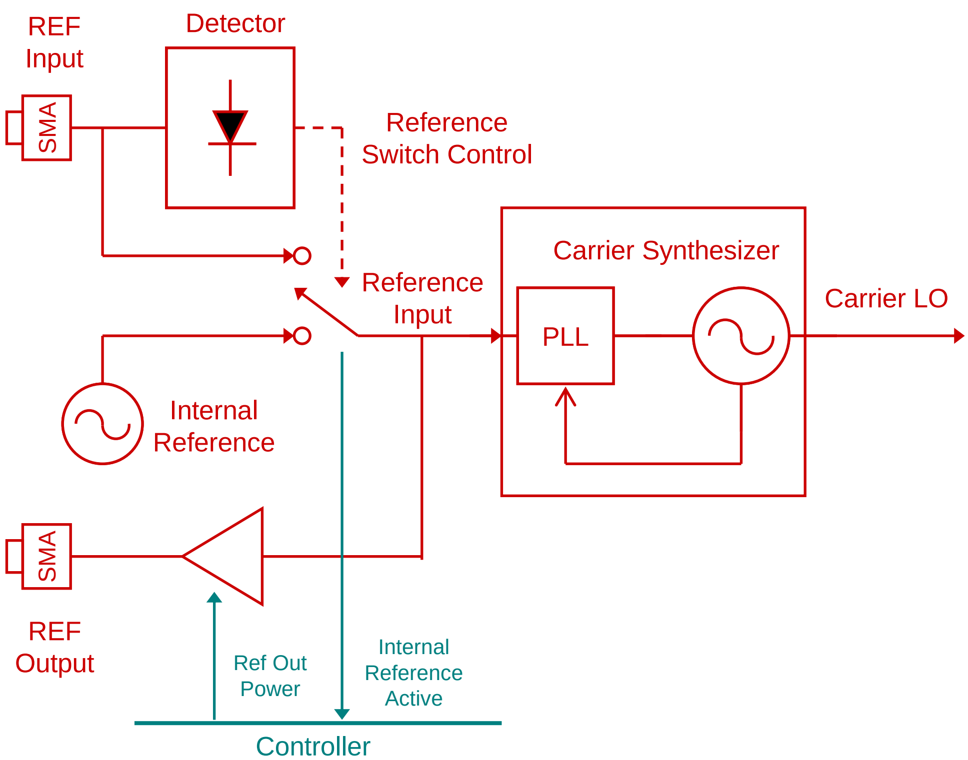


Figure 6-10 Carrier LO Reference Source Diagram

6.2.4 Carrier LO Source Selection

There are three options for the quadrature modulator LO source: external carrier, internal carrier and divided internal carrier as shown in Figure 6-11. Users can supply their own LO by applying a signal to the reference input SMA. The reference input port is continuously monitored for power level by an on-board power detector. Once the power level crosses a given threshold the LO source switch is set to select the external carrier as the LO source. The external LO status is available to the user through the on-board controller.

Provided there is no external source detected at the reference input, the user has the option of choosing between the internal carrier and the divided internal carrier using the divider select command. The divided internal carrier source is automatically selected when the divider is enabled. The user must disable the divider if an external carrier source is applied to the source input connector.

☞	The clock divider must be disabled when using an external source for the carrier LO.

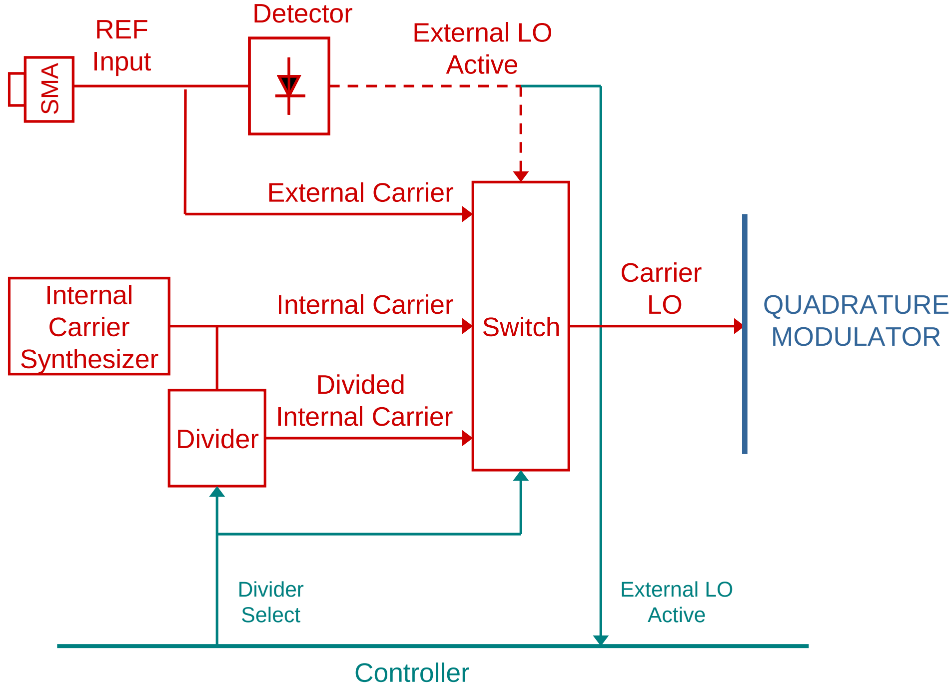


Figure 6-11 Carrier LO Source Diagram

6.3 Quadrature Modulator and RF Output Chain

A block diagram of the quadrature modulator and RF output chain is shown in Figure 6-12. The carrier LO is modulated by analog data from the baseband inputs and the modulator output is fed through a variable attenuator and RF amplifier chain for level control. The following paragraphs describe the quadrature modulator and RF output chain functions.

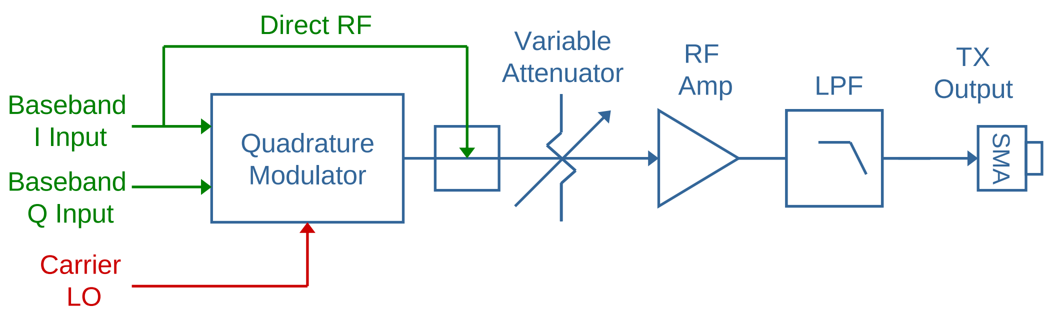


Figure 6-12 Modulator and RF Output Diagram

6.3.1 Quadrature Modulator

The quadrature modulator combines the I and Q input data streams with the carrier LO to create a modulated carrier. The resulting waveform is buffered and output through the RF output port as shown in the block diagram of Figure 6-13. The device used for quadrature modulation is listed in the key components section of the manual in section 6.5.

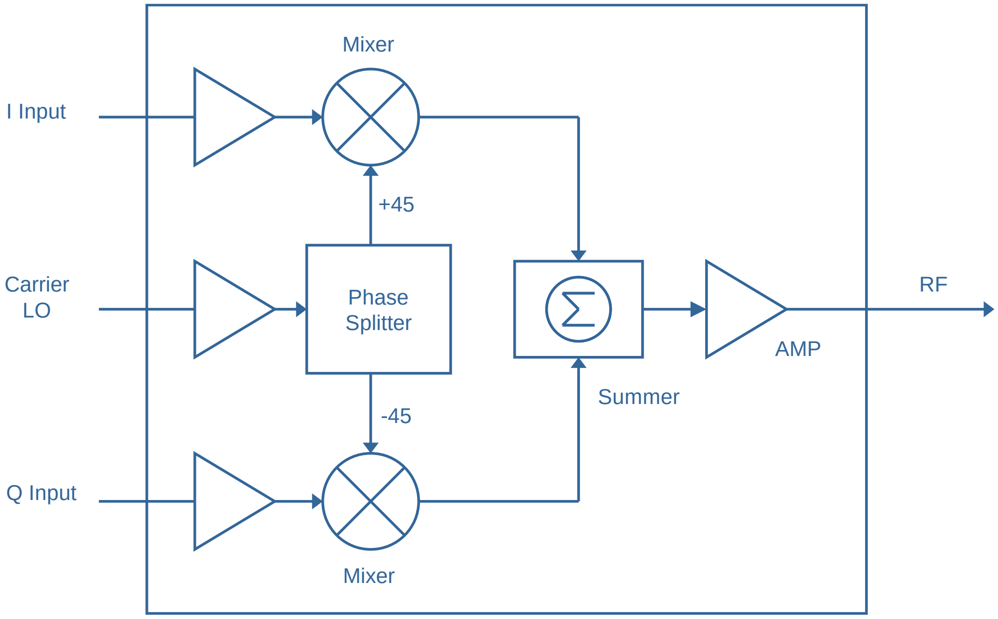


Figure 6-13 Quadrature Modulator block diagram

6.3.2 RF Output Chain

The Model 150 RF chain consists of the signal path that runs from the modulator output to the TX output SMA. The chain consists of a direct RF switch, variable attenuator, RF amplifier and fixed lowpass filter as shown in the block diagram of Figure 6-14. Full RF output power is achieved when the baseband I and Q inputs are at their maximum levels and the variable attenuator is set to its lowest value. Output power can be modified by the user in discrete steps under software control by changing the value of the variable attenuator. Finer control over the amplitude level can be obtained by varying the amplitude of the baseband I and Q inputs. The output power of the RF chain varies by several dB over the full frequency range of the unit due to path and component losses at high frequencies. A lowpass filter resides at the end of the chain to reduce broadband amplifier noise and limit higher order harmonics. See section 3.0 for input/output level and attenuator step size/range information. Section 5.0 contains performance characterization data including the transmitter frequency response.

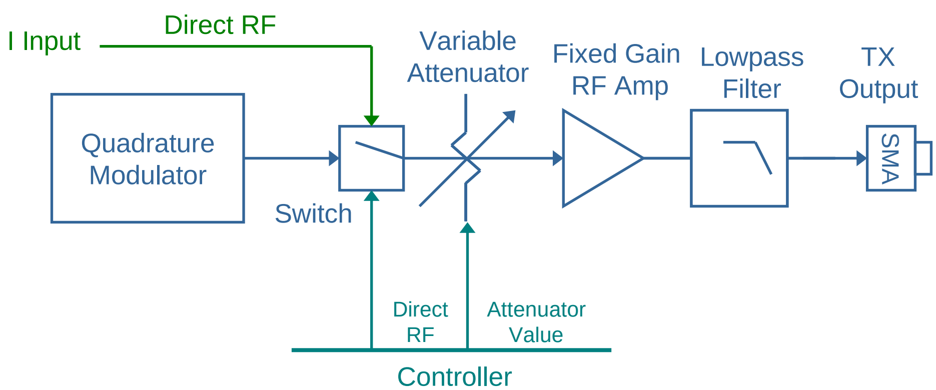


Figure 6-14 RF Output Chain Diagram

The baseband I input can be routed directly to the RF output chain by setting the direct RF mode switch. A detailed description of the direct RF mode of operation can be found in section 6.1.4.

6.4 Board Controller

The controller provides a gateway from the express bus interface to the command/status functions of the Model 150 hardware. The controller resides on the PCI express bus as a single lane endpoint and provides connectivity to the hardware as shown in Figure 6-15. The controller receives user command/status requests over the PCI express bus and routes them to the serial bus interface or converts them into discrete signal command/status requests. Red Rapids provides an API that allows users to communicate via software with the Model 150 using simple read and write commands. More information on the user/controller interface can be found in the *Wavefront Software Manual*.

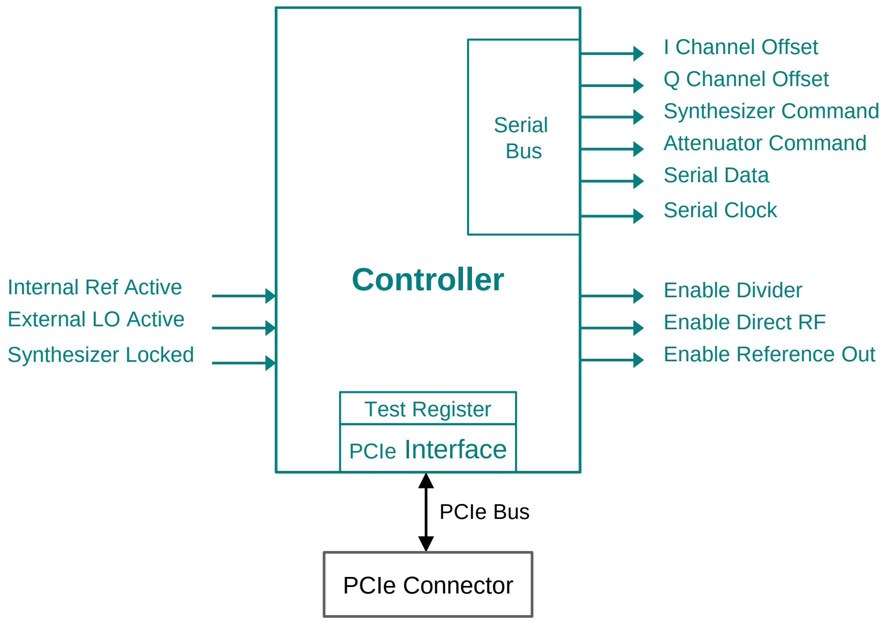


Figure 6-15 Controller Block Diagram

6.5 Key Components

The key hardware components for the Model 150 assembly are listed in Table 6-1. This information is supplied to assist in the development of custom application code.

Table 6-1 Key Hardware Components

Component	Part Number	Vendor	Comments
Voltage Offset DAC	LTC1661	Linear Tech	Dual 10-bit DAC
Quadrature Modulator	HMC497LP4	Hittite Microwave	100-4000MHz Quadrature Modulator
Attenuator	HMC624LP4	Hittite Microwave	6-bit Digital Attenuator

7.0 External Interfaces

7.1 Front Panel Interface

There are five SMA coaxial connectors and four LEDs located along the face of the Model 150 module as shown in Figure 7-1. Connector and LED functions are listed in Table 7-1. Operating levels and specifications for all I/O functions can be found in section 3.0.

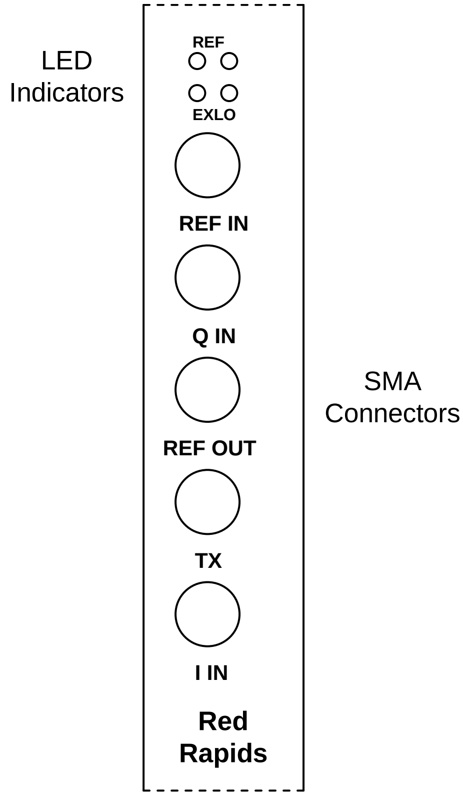


Figure 7-1 Model 150 Front Panel Connectors

Table 7-1 Front Panel Connectors

Des	Label	Connector	I/O	Description
D3A	REF (A)	LED Yellow	-	External Reference Active
D3B	REF (B)	LED Green	-	Internal Reference Active
D4A	EXLO (A)	LED Yellow	-	External Carrier LO Active
D4B	EXLO (B)	LED Green	-	Internal Carrier LO Active
J1	REF IN	SMA	I	Reference/LO Input Port
J2	Q IN	SMA	I	Baseband Q Input Port
J3	REF OUT	SMA	O	Reference Output Port
J4	TX	SMA	O	RF Output
J5	I IN	SMA	I	Baseband I Input Port

7.2 Host Interface

The host interface for the Model 150 is the PCI express bus and is completely specified by the documents listed in section 1.2. The Model 150 operates as a single lane endpoint but uses a four lane form factor for thermal and mechanical reasons. Table 7-2 lists the Model 150 board connectivity to PCI Express connector.

Table 7-2 PCI Express Interface Connections (1)

Name	Side B	Connection	Connection	Side A	Name
+12V	1	Y	Y	1	PRSNT1#
+12V	2	Y	Y	2	+12V
+12V	3	Y	Y	3	+12V
GND	4	Y	Y	4	GND
SMCLK	5	NC	NC	5	JTAG2
SMDAT	6	NC	NC	6	JTAG3
GND	7	Y	NC	7	JTAG4
+3.3V	8	Y	NC	8	JTAG5
JTAG1	9	NC	Y	9	+3.3V
3.3Vaux	10	CAP	Y	10	+3.3V
WAKE#	11	Y	Y	11	PERST#
RSVD	12	NC	Y	12	GND
GND	13	Y	Y	13	REFCLK+
PETp0	14	Y	Y	14	REFCLK-
PETn0	15	Y	Y	15	GND
GND	16	Y	Y	16	PERp0
PRSNT2#	17	NC	Y	17	PERn0
GND	18	Y	Y	18	GND
PETp1	19	NC	NC	19	RSVD
PETn1	20	NC	Y	20	GND
GND	21	Y	NC	21	PERp1
GND	22	Y	NC	22	PERn1
PETp2	23	NC	Y	23	GND
PETn2	24	NC	Y	24	GND
GND	25	Y	NC	25	PERp2
GND	26	Y	NC	26	PERn2
PETp3	27	NC	Y	27	GND
PETn3	28	NC	Y	28	GND
GND	29	Y	NC	29	PERp3
RSVD	30	NC	NC	30	PERn3
PRESNT2#	31	Y	Y	31	GND
GND	32	Y	NC	32	RSVD

Notes:

(1) The abbreviations for connections are as follows: Y – connected per specification, NC – not connected, CAP – Capacitor to ground

7.2.1 Board LED Indicators

There are two LED indicators that report ancillary hardware status functions as listed in Table 7-3. These LEDs are not visible from the front panel.

Table 7-3 LED Operating Status Indicators

Reference Designator	Color	Status (Illuminated)
D1	Red	Synthesizer unlocked
D2	Green	Board power good

The board LED locations are shown in Figure 7-2.

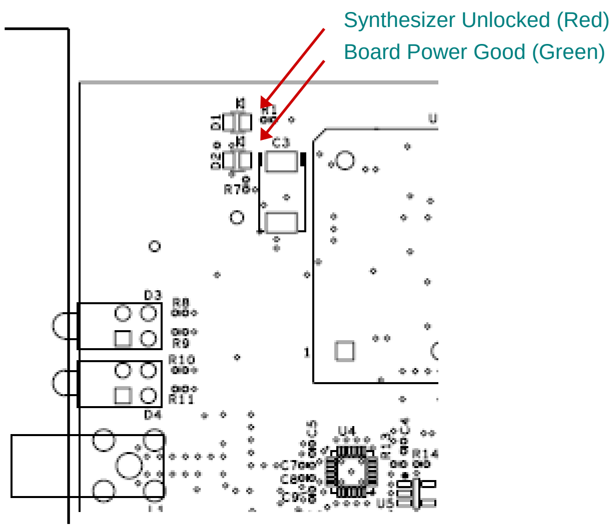


Figure 7-2 Board Diode Locations

8.0 Build Options

Red Rapids offers several build options to help users tailor the performance of the model 150 to their application. Table 8-1 provides as list of options for the internal synthesizer frequency range. The frequency sub-bands and no synthesizer options are available at a reduced cost for users not requiring the full operating (250 – 4000 MHz) band. Custom synthesizer frequencies are also available please contact Red Rapids for details.

Table 8-1 Internal Synthesizer Build Options

	Full	UHF	L-Band	S-Band	None	Custom
Internal Synthesizer Range (MHz)	250-4000	250-1000	1000-2000	2000-4000	No Synth	Custom

The internal reference is available as a low cost TCXO or high stability OCXO option as shown in Table 8-2.

Table 8-2 Internal Reference Build Options

Internal Reference	TCXO	OCXO

Red Rapids offers custom filters for the baseband input and direct RF mode paths. The standard filter types and cutoffs are displayed in Table 8-3. Frequency response plots for the standard filters can be found in section 6.1.

Table 8-3 Model 150 Standard Filter Configurations

Path	Type	Order	Cutoff (3dB)
Baseband Input	Chebyshev	5^{th}	45MHz
Direct RF	Elliptical, C07 20 theta = 40	7^{th}	150MHz

The Model 150 can be ordered with different filter options as listed in Table 8-4. Please contact Red Rapids technical support with your requirements.

Table 8-4 Model 150 Build Options[1]

Item	Options
Filter Topology	Butterworth Chebyshev Elliptical[1]
Filter Type	Lowpass Highpass
Order **Baseband** **Direct RF**	 3, 5 3, 5, 7
Frequency Range[2]	10 - 750 MHz

Note: [1]Elliptical not available for baseband filters.
[2]Some filter implementations may not realizable due to component limitations.

Some filter implementations cannot be supported due to component limitations. Please check with Red Rapids prior to ordering.

Delivery lead times are subject to component availability at time of order.

9.0 Technical Support

Please feel free to contact us if you have a technical question about or problem with our product. We understand that our customers have tight deadlines and time is of the essence in development and production cycles. We will make every effort to resolve problems as quickly as possible.

Web: www.redrapids.com

Email: support@redrapids.com

Phone: 972-671-9570

Fax: 972-671-9572

Please include the following information with your correspondence:

Contact Information

Product Model

Host System (PC type)

Operating System

Problem Description