

SigStream™

Quick Start Guide



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1.0 Introduction

The SigStream™ product family transforms a general purpose computer into a high speed signal acquisition/generation platform. The hardware incorporates a rich set of software programmable features that include selectable operating modes, external or timed event triggers, timestamped data samples, and flexible data formatting. The software configurable datapath can be tailored to process a variety of signal types from radio waveforms to instrumentation.

The latest product documentation and software is available for download from the Red Rapids web site (www.redrapids.com).

1.1 Model Number Options Decoder

The SigStream™ product family offers several analog interface options coupled to a common digital signal processing architecture. Each product is assigned a six-digit model number (Model XXX-YYY) that uniquely identifies the specific hardware features of that unit. The first three digits are the primary designator used to convey information about the structure of the analog front-end. The last three digits define the build options selected by a customer to tailor the product to a specific application. Consult the SigStream™ Model Number Options Decoder manual (REF-007-002-Rxx) for a current list.

1.2 Conventions

This manual uses the following conventions:

- Hexadecimal numbers are prefixed by “0x” (e.g. 0x00058C).
- **Blue** font is used for names of directories, files and OS commands.
- **Green** font is used to designate source code.



Text in this format highlights useful or important information.



Text shown in this format is a warning. It describes a situation that could potentially damage your equipment. Please read each warning carefully.

The following are some of the acronyms used in this manual.

- **ADC** Analog to Digital Converter
- **API** Application Program Interface
- **CCXMC** Conduction Cooled Express Mezzanine Card
- **CLK** External Clock
- **DAC** Digital to Analog Converter
- **DEV#** Device Number #
- **GPIO** General Purpose I/O
- **LED** Light Emitting Diode
- **PCIe** Peripheral Component Interconnect Express
- **REF** External 10 MHz Clock Reference
- **RX** Receiver
- **TOD** Time of Day
- **TX** Transmitter

- **TOD** Time of Day
- **TRIG** External Trigger
- **XMC** Express Mezzanine Card

1.3 Distribution Disk (DSK-270-001-Rxx)

The demonstration software and SigStream™ API are distributed on Red Rapids disk archive number DSK-270-001-Rxx. The directory structure of the archive is outlined below:

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The root directory contains three files that are used to compile the demonstration source code. The [VSbuild-32.bat](#) and [VSbuild-64.bat](#) batch files can be executed from a Visual Studio command prompt to build the 32-bit or 64-bit Windows executable. The [makefile](#) will compile either the 32-bit or 64-bit Linux to match the installation. The [sigstream.c](#) main function is also located in the root directory.

[\files](#)

The [files](#) subdirectory contains an example of a frame descriptor file ([frame.txt](#)) used by the scheduler and a waveform source file ([waveform.txt](#)) used to source transmitter samples to the demonstration.

[\filters](#)

The [filters](#) subdirectory contains configuration files for each type of filter available in a SigStream™ datapath. The filenames take the form [filter<M>_type<N>.txt](#), where M is the filter number in the channel and N is the type number.

[\include](#)

The [include](#) subdirectory contains the header file used to access the SigStream™ API.

[\linux_x86-32](#)

The [linux_x86-32](#) subdirectory is the repository for object and executable files generated when the [makefile](#) is executed from a 32-bit Linux installation. It is also the destination for output files created when the demonstration application is run.

[\linux_x86-64](#)

The [linux_x86-64](#) subdirectory is the repository for object and executable files generated when the [makefile](#) is executed from a 64-bit Linux installation. It is also the destination for output files created when the demonstration application is run.

[\src](#)

The [src](#) subdirectory contains source code to all SigStream™ API functions.

[\win_x86-32](#)

The [win_x86-32](#) subdirectory is the repository for object and executable files generated when the [VSbuild-32.bat](#) batch file is executed. It is also the destination for output files created when the demonstration application is run. This subdirectory includes a [Set_Path.bat](#) batch file that can be used to add the driver directory (DSK-806-902-Rxx) to the Windows search path.

[\win_x86-64](#)

The [win_x86-64](#) subdirectory is the repository for object and executable files generated when the [VSbuild-64.bat](#) batch file is executed. It is also the destination for output files created when the demonstration application is run. This subdirectory includes a [Set_Path.bat](#) batch file that can be used to add the driver directory (DSK-806-902-Rxx) to the Windows search path.

1.4 Revision History

Version	Date	Description
R00	2/1/2018	Initial release.

2.0 Software Installation

The SigStream™ software suite consists of three disk archives:

DSK-806-902-Rxx: Adapter Device Driver and API

DSK-270-001-Rxx: Demonstration Software and SigStream™ API

DSK-806-066-Rxx: Flash Programmer

The software is available for download from the Red Rapids website (www.redrapids.com). Each archive is accompanied by a reference manual that describes the function and operation of the software distributed on that disk.

The distribution number of each archive is also the name of the root directory for that disk. All three archives must be extracted into the same working directory so that they share a common folder on the host. This is necessary for path names between the subdirectories to cross reference correctly.

The Adapter Device Driver needs to be installed on the host computer before any application will execute.

The demonstration software consists of the SigStream™ API and an application example that demonstrates all API functions. There is no special installation procedure required.

The Flash Programmer is a utility used to load firmware updates as they become available. All firmware revisions are available from the Red Rapids website (www.redrapids.com).

3.0 Hardware Installation

Every SigStream™ product is available in both XMC and PCI Express (PCIe) half-length form factors. The hardware ships with a x8 physical and x8 electrical PCIe connector. It is possible to load alternate firmware that reduces the number of electrical connections if desired.

3.1 XMC Hardware Installation

The following instructions provide a general guide for mounting a XMC module to a baseboard or carrier host socket. Consult your baseboard documentation for product specific guidance.



This is a static sensitive electronic device; please follow standard ESD guidelines when installing the device.

Load Drivers: Load the appropriate software drivers prior to installing the hardware.

Power Down: Power to the host must be off during hardware installation. Permanent damage may result if the card is plugged into a hot socket.

Identify Socket: Find an open XMC socket on the host. The socket may be keyed for legacy PMC operation. The key consists of a metal post located at the centerline of the socket between the electrical connectors. The position of the post will indicate if the legacy PCI bus is designed for 3.3 Volt or 5 Volt signaling. The SigStream™ XMC product does not support legacy PCI operation, but the card is designed to accommodate a 3.3 Volt key for convenience.

Insert Card: Angle the XMC bezel into the host front panel cut-out. The EMI gasket around the bezel may offer resistance, be careful not to dislodge the gasket from the groove. Gently press the XMC down onto the host until the connectors mate.

Secure Card: Secure the XMC hardware with four mounting screws (provided). Be sure that the card does not bow as the screws are fastened.

Check Obstructions: Verify that the card is securely mounted in the XMC socket and not in contact with other components on the host.

Boot Computer: The host will detect the presence of new hardware the first time power is applied. Consult the driver installation instructions if prompted for additional information.



The expansion card can pick up electrical interference from other devices or directly through the host power supply. Try moving the card away from other devices or try a different host platform if you are experiencing interference.

3.2 PCIe Hardware Installation

The following instructions provide a general guide for PCIe expansion card installation. Consult your host documentation for product specific guidance.



This is a static sensitive electronic device; please follow standard ESD guidelines when installing the device.

Load Drivers: Load the appropriate software drivers prior to installing the hardware.

Power Down: Power to the host must be off during hardware installation. Permanent damage may result if the card is plugged into a hot socket.

Identify Slot: Find an open PCIe slot on the host backplane and verify that the socket is compatible with the card you are installing. The PCI Express specification defines each slot by a physical size and electrical size. It is not uncommon to find a socket electrically wired to fewer lanes than the physical size allows. The specific configuration is usually silkscreened on the motherboard.

The interoperability of PCIe cards and slots is summarized in Table 3-1. The SigStream™ card ships with a x8 physical connector.

Table 3-1 PCIe Card Interoperability

Slot	x1	x4	x8	x16
Card				
x1	Required	Required	Required	Required
x4	No	Required	Allowed	Allowed
x8	No	No	Required	Allowed
x16	No	No	No	Required

Remove Metal Insert: The expansion slot opening will typically be covered by a metal insert held in with a single screw. The metal insert may have to be punched out of some cases. Unscrew or punch out the appropriate metal insert. It may help to align the expansion card over the slot to determine which insert to remove.

Insert Card: Align the expansion card edge connector with the PCIe slot making sure the bottom edge of the metal faceplate clears the edge of the backplane motherboard. Apply firm pressure to seat the card in the slot. You may need to rock the card slightly from front to back to get the unit seated properly. *Do not force the card or significantly flex the motherboard.* The expansion board should not require much force to insert provided everything is lined up correctly.

Secure Card: The top side of the faceplate should be flush or close to flush with the card retention bar. If the plate is not close to the bar, verify that the board is not canted in the slot. Secure the expansion card to the chassis by inserting a screw into the top of the metal faceplate.

Check Obstructions: Verify that the card is securely mounted in the PCIe slot and not in contact with other items inside the chassis.

Boot Computer: The host will detect the presence of new hardware the first time power is applied. Consult the driver installation instructions if prompted for additional information.

 The expansion card can pick up electrical interference from other devices or directly through the host power supply. Try moving the card away from other devices or try a different host platform if you are experiencing interference.

4.0 Front Panel Connectors

The face of each SigStream™ product contains an array of coaxial and digital connectors to connect signals, clocks and external triggers. If a bezel or face plate is present, each connector will be marked with one of the following designators:

RX#: Analog receiver channel number # input.

TX#: Analog transmitter channel number # output.

GPIO: General purpose I/O connector for external triggers.

REF/CLK: External 10 MHz reference or sample clock input.

TRIG: Coaxial trigger input or 1 PPS timing input.

There are two light emitting diodes (LEDs) located on either side of the GPIO connector. The yellow LED illuminates when the active edge of the selected trigger is detected and the green LED illuminates when any channel is actively processing data.

The connector placement and LED location for each product is shown below. The three available form factors are illustrated for each product.

4.1 Model 271

The Model 271 front panel includes four coaxial connectors and one GPIO connector as shown in Figure 4-1. The coaxial receiver channel inputs are numbered RX1 and RX2. The remaining two coaxial connectors are the REF/CLK input and TRIG input.

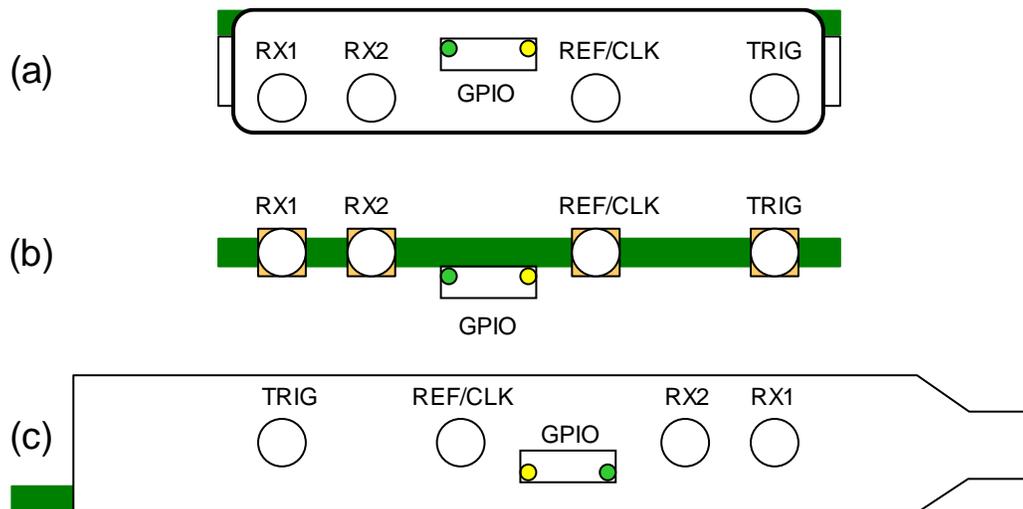


Figure 4-1 Model 271 (a) XMC, (b) CCXMC, (c) PCIe Front Panel

4.2 Model 272

The Model 272 front panel includes five coaxial connectors and one GPIO connector as shown in Figure 4-2. The coaxial receiver channel inputs are numbered RX1 and RX2, while the transmitter outputs are numbered TX3 and TX4. The fifth coaxial connector can either be used as a REF/CLK input or a TRIG input.

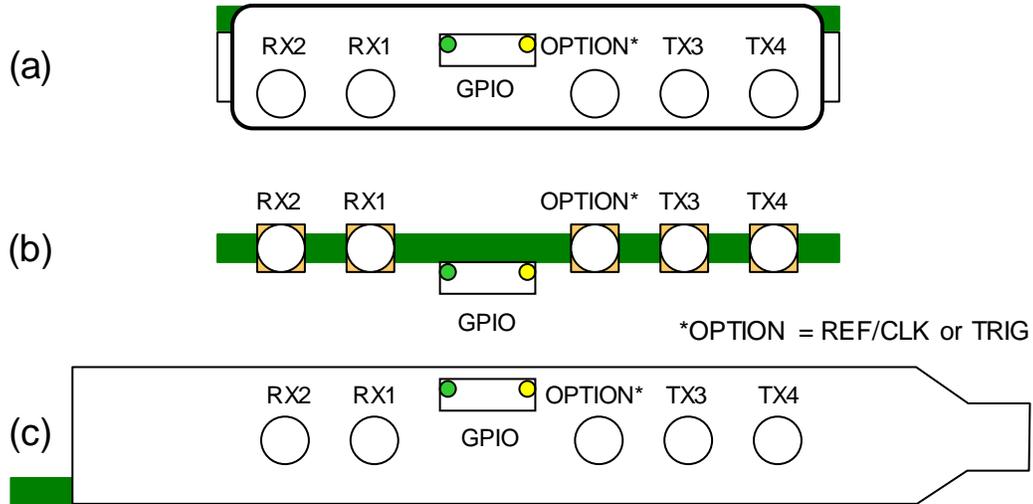


Figure 4-2 Model 272 (a) XMC, (b) CCXMC, (c) PCIe Front Panel

4.3 Model 273

The Model 273 front panel includes four coaxial connectors and one GPIO connector as shown in Figure 4-3. The coaxial receiver channel inputs are numbered RX1 and RX2. The remaining two coaxial connectors are the REF/CLK input and TRIG input.

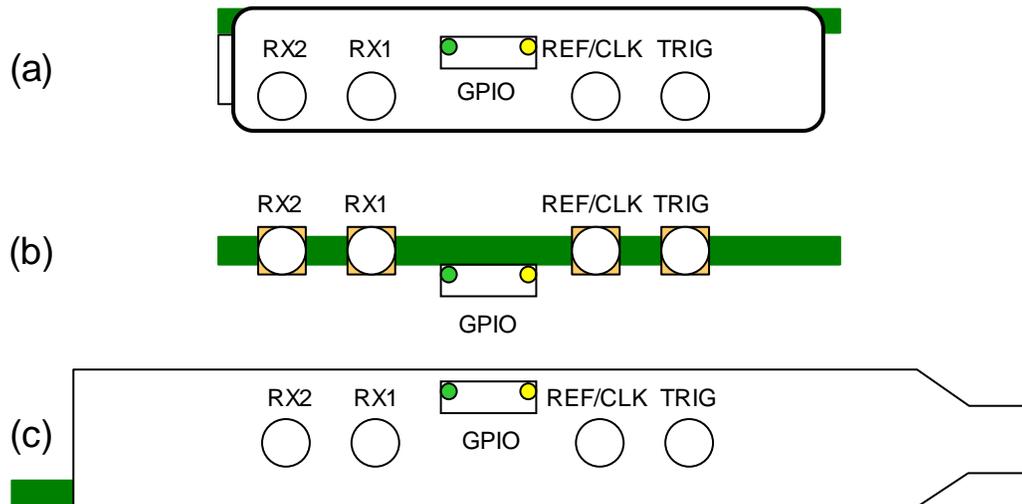


Figure 4-3 Model 273 (a) XMC, (b) CCXMC, (c) PCIe Front Panel

4.4 Model 274

The Model 274 front panel includes four coaxial connectors and one GPIO connector as shown in Figure 4-4. The coaxial transmitter channel outputs are numbered TX1 and TX2. The remaining two coaxial connectors are the REF/CLK input and TRIG input.

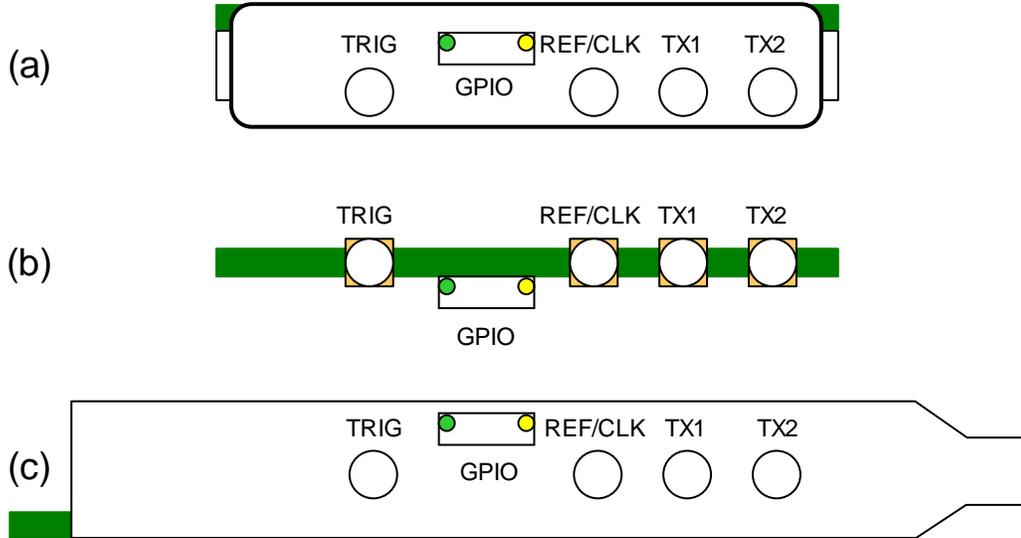


Figure 4-4 Model 274 (a) XMC, (b) CCXMC, (c) PCIe Front Panel

4.5 Model 276

The Model 276 front panel includes three coaxial connectors and one GPIO connector as shown in Figure 4-5. The coaxial receiver channel input is labeled RX1. The remaining two coaxial connectors are the REF/CLK input and TRIG input.

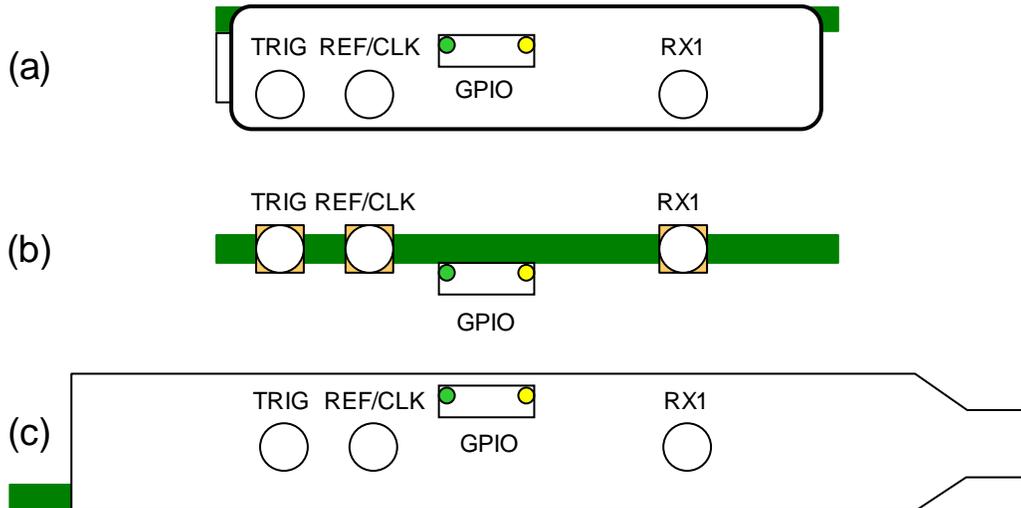


Figure 4-5 Model 276 (a) XMC, (b) CCXMC, (c) PCIe Front Panel

4.6 Model 277

The Model 277 front panel includes five coaxial connectors and one GPIO connector as shown in Figure 4-6. The coaxial receiver channel inputs are consecutively numbered RX1 through RX4. The fifth coaxial connector can either be used as a REF/CLK input or a TRIG input.

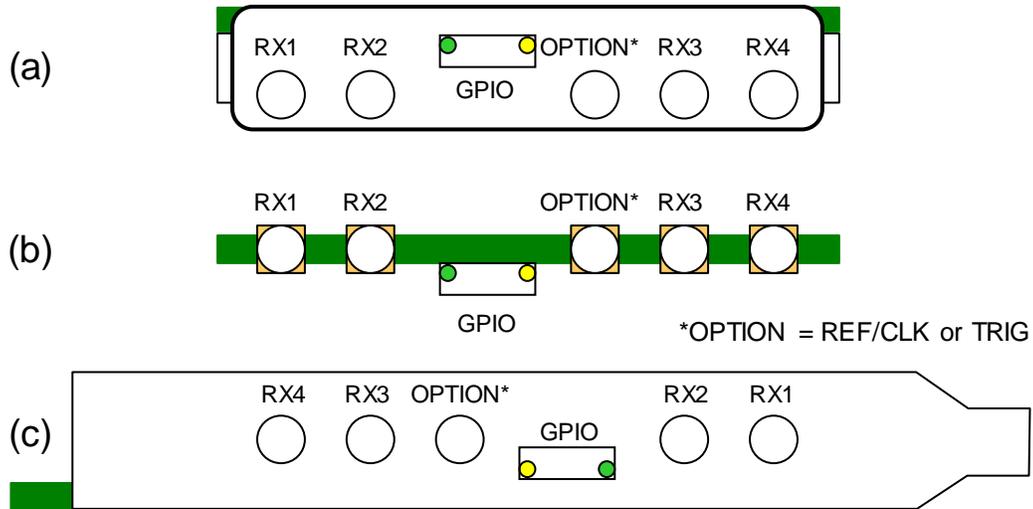


Figure 4-6 Model 277 (a) XMC, (b) CCXMC, (c) PCIe Front Panel

5.0 Hardware/Software Demonstration

Each SigStream™ product is accompanied by a software application that demonstrates hardware functionality using calls to the supplied API. Products equipped with receiver channels will digitize an analog signal, transfer samples to host memory using DMA transactions, and store a snapshot of the collection to a text file. Products equipped with transmitter channels will retrieve digital samples from host memory via DMA transactions and produce an analog reproduction of the digital signal. The samples originate from a text file containing a waveform snapshot that is copied to host memory by the application before transmission begins.

The demonstration software is provided on software archive DSK-270-001-Rxx. The application can be run from a command prompt by executing the following instructions from the root directory.

32-bit Linux	64-bit Linux	32-bit Windows	64-bit Windows
> make	> make	> cd win_x86-32	> cd win_x86-64
> cd linux_x86-32	> cd linux_x86-64	> Set_Path	> Set_Path
> ./sigstream	> ./sigstream	> sigstream	> sigstream

5.1 Receiver Demonstration

Figure 5-1 illustrates the hardware path exercised by the receiver demonstration software. The application enables all available channels and issues a software trigger to initiate signal acquisition.

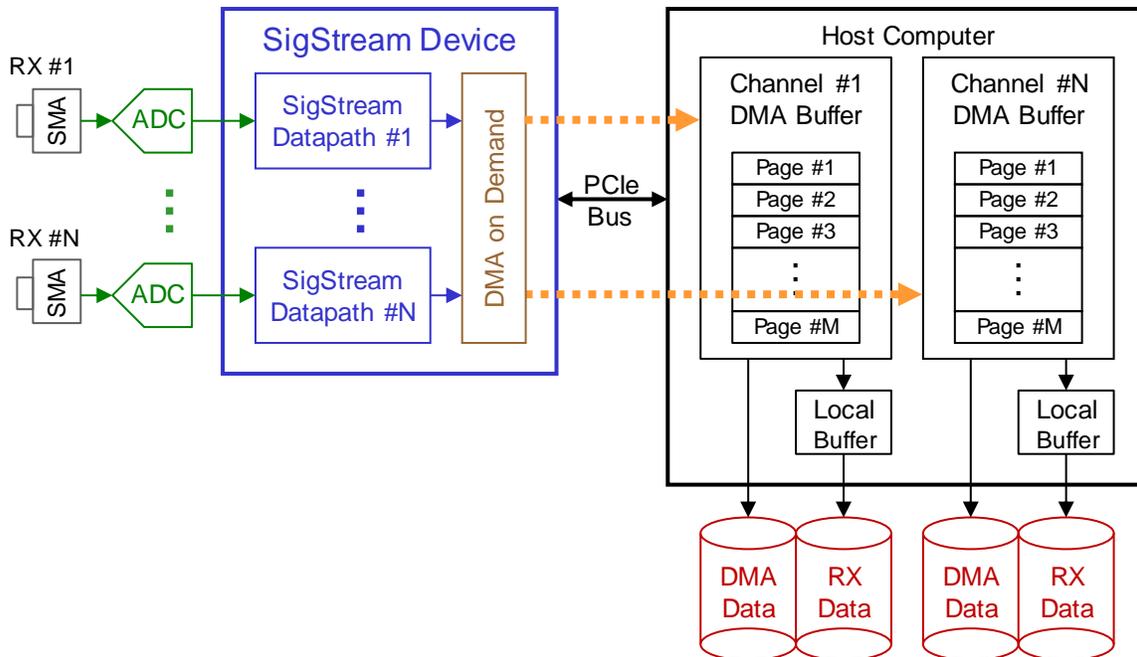


Figure 5-1 Receiver Data Flow

The SigStream™ datapath processes the number of samples requested by the channel configuration. All channels are configured identically for demonstration purposes. Refer to

the SigStream™ Operating Guide (REF-004-002-Rxx) for details about channel configuration variables.

Each channel continuously writes digital data samples to a dedicated DMA buffer in host memory. The DMA transactions are mastered by the SigStream™ device, no software intervention is required. Consult the DMA on Demand Operating Guide (REF-004-000-Rxx) for further details about DMA transactions. The application software continuously transfers the contents of each DMA buffer to another local memory buffer to demonstrate how a customer application would manage the incoming data.

The demonstration will create two output files per channel. The first set of files are named `dma#buf.txt`, where # is the channel number. This file contains the first page of sample data in the DMA buffer. The number of pages that are written to the file can be changed in the call to the `DMA Save()` API function, but must not be any greater than the total number of pages in the DMA buffer. The second set of files are named `rx#data.txt`, where # is the channel number. This file contains the first page of sample data stored in the local buffer. The number of pages written can be increased, but must not be any greater than the number of pages between DMA markers. The data in the `rx#data.txt` and `dma#buf.txt` files will only match if processing terminated while writing to a DMA page number between the first and second DMA marker.

No external equipment is required to run the demonstration code, but the receiver channels will only collect noise samples if there is no input signal present. Each SigStream™ product is assigned an analog Front End Reference Manual (REF-000-YYY-Rxx) that contains information about the expected input signal power.

5.2 Transmitter Demonstration

Figure 5-2 illustrates the hardware path exercised by the transmitter demonstration software. The application enables all available channels and issues a software trigger to initiate signal generation.

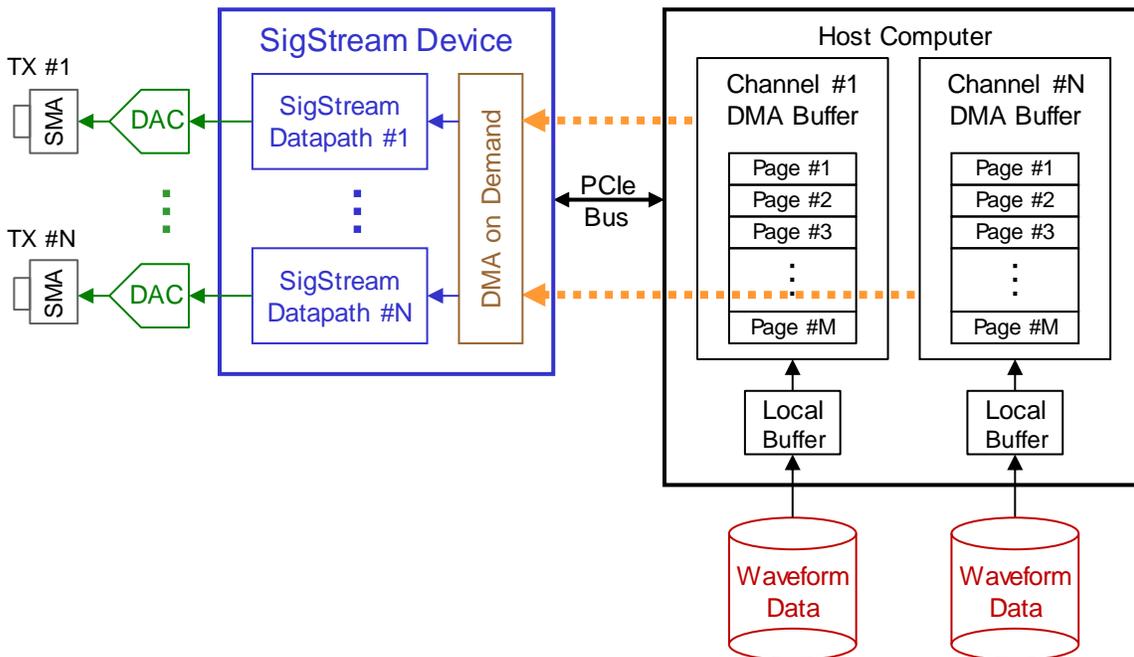


Figure 5-2 Transmitter Data Flow

The SigStream™ datapath processes the number of samples requested by the channel configuration. All channels are configured identically for demonstration purposes. Refer to the SigStream™ Operating Guide (REF-004-002-Rxx) for details about channel configuration variables.

The demonstration software loads digital samples from the [waveform.txt](#) file into a local memory buffer before the channels are enabled. Once processing begins, the application continuously transfers the contents of the local buffer to a DMA buffer to demonstrate how a customer application would supply outgoing data. The SigStream™ device continuously reads samples from the DMA buffer in host memory and supplies them to the datapath. The DMA transactions are mastered by the SigStream™ device, no software intervention is required. Consult the DMA on Demand Operating Guide (REF-004-000-Rxx) for further details about DMA transactions.

It is important to note that the waveform stored in the local buffer does not get updated once channel processing begins. The same block of samples will be repeated through the datapath if the requested number of samples exceeds the size of the local buffer. This will result in phase discontinuities if the final waveform sample does not represent the end of a period.

The demonstration will create one output file per channel named [tx#probe.txt](#), where # is the channel number. This file contains the first 1024 samples entering the DAC following the software trigger. It is provided as a debug tool to verify that the channel is producing the expected digital output signal.

No external equipment is required to run the demonstration code, but a spectrum analyzer can be used to monitor the output waveform of each channel. Each SigStream™ product is assigned an analog Front End Reference Manual (REF-000-yyy-Rxx) that contains information about the expected output signal power.

5.3 Transceiver Demonstration

SigStream™ products that are equipped with both receiver and transmitter channels will run both demonstrations concurrently. A single software trigger will initiate processing on all channels simultaneously, regardless of direction.

6.0 Run-time Messages

The SigStream™ application reports status, warning, and error messages to the screen as it executes. Appendix 7.0 contains an example report that was generated by a system equipped with both receiver and transmitter devices.

6.1 Open Device

Three messages are generated when a hardware device is successfully opened by the application.

- (1) Firmware revision reported by the hardware.
- (2) Model number reported by the hardware.
- (3) Clock status.

The first two messages simply convey information to identify the hardware. The third message reports the health of the clock network and the specific clock source detected by the hardware. This message will change depending on whether there is an external reference or external sample clock connected through the front panel. An error will be reported if any type of clock problem is detected.

6.2 Load Configuration Settings

The on-board time of day (TOD) clock is reset to zero during the configuration process. That value is then read back from the hardware and reported in a message to verify that it is correct.

Every available channel on the SigStream™ device is loaded with individual configuration settings. A status message is generated as each channel completes.

6.3 PCIe Performance Benchmark

It is important to know whether the host computer can supply the PCIe bus bandwidth required by a SigStream™ device. A performance test is run by the application to measure actual performance with all available channels continuously making DMA requests. The number reported by the benchmark must be above the expected throughput of the device to avoid losing data.

The performance benchmark is only provided for convenience, it can be eliminated from the code once the information is collected.

6.4 Enable Channels

A message is generated as every channel on the device is enabled in sequence. Channel processing does not begin immediately, the channels are simply armed and waiting for the requested trigger.

6.5 Start/Stop Processing

A software trigger is issued to start processing samples on all channels simultaneously. The application waits silently for each channel to complete the requested number of samples and stop. Terminating the process while the channels are active (CTRL-C) may crash the computer since the hardware is still accessing protected DMA buffer space in host memory.

The demonstration software copies fresh data out of the receiver DMA buffers into local memory while the channel is active. Similarly, fresh data is copied into the transmitter

DMA buffers. The DMA buffers can be monitored by either polling the status bits or waiting for an interrupt. The demonstration software defaults to polling.

6.6 Retrieve Temperature and Power Status

There are multiple temperature sensors and power monitors available on the SigStream™ device. The application queries all available sensors and reports the results when processing is complete. Any temperature above 90 degrees C indicates inadequate cooling for the hardware.

6.7 Review Channel Status

There are several error conditions monitored by the device throughout operation. These are reviewed and reported when channel processing completes.

- (1) Read or write to an illegal BAR address.
- (2) Loss of stable clocks.
- (3) ADC over-range.
- (4) FIFO overflow (receiver) or underflow (transmitter).
- (5) Loss of DMA data.

The first message simply indicates that software issued a PCIe read or write command to a register address that does not exist in the hardware. A clock error would only occur if there were some type of hardware event that causes a clock to lose lock. The ADC over-range occurs when the input signal exceeds the maximum amplitude supported by the device, but it is worth noting that not all ADC chips offer this status. A FIFO error will usually occur when the PCIe bus is not fast enough to meet the throughput demands of all active channels competing for resources. A loss of DMA data indicates that the software servicing the DMA buffers in host memory is not fast enough to keep up with the refresh rate demanded by the hardware. This might be resolved by increasing the size of the DMA buffers or changing the number of pages between markers. However, it is always possible that the host processor is simply not fast enough to keep up with the transfer of data between the device and host.

6.8 Save Captured Data (RX Only)

Every receiver channel will produce two text files as discussed in Section 5.1. Both files will contain signed integer values. A real data sample occupies a single line in the file while a complex sample occupies two lines. The real (in-phase) value always precedes the imaginary (quadrature) value of a complex sample. The maximum allowed positive or negative value is dictated by the data item size selected in the channel configuration.

6.9 Save Probe Data (TX Only)

Every transmitter channel will produce one text files as discussed in Section 5.2. The file will contain signed integer values. A real data sample occupies a single line in the file while a complex sample occupies two lines. The real (in-phase) value always precedes the imaginary (quadrature) value of a complex sample. The maximum allowed positive or negative value is dictated by the data item size selected in the channel configuration.

7.0 Appendix A – Example Run-time Report

The following output messages were produced by the SigStream™ application running on a host computer with a Model 277 receiver (DEV0) and Model 274 transmitter (DEV1) installed on the PCIe backplane.

***** SigStream™ *****

Initializing structures...

Opening DEV0 on the host...

Firmware revision (MMDDYYYY): 12012017
Initializing Red Rapids Model 277.
Sample clock locked to internal reference, digital clocks locked.

Opening DEV1 on the host...

Firmware revision (MMDDYYYY): 12012017
Initializing Red Rapids Model 274.
Sample clock locked to internal reference, digital clocks locked.

Loading DEV0 configuration settings...

Current time of day (TOD) setting: 0 seconds
Channel #1 configuration loaded.
Channel #2 configuration loaded.
Channel #3 configuration loaded.
Channel #4 configuration loaded.

Loading DEV1 configuration settings...

Current time of day (TOD) setting: 0 seconds
Channel #1 configuration loaded.
Channel #2 configuration loaded.

Measuring the DEV0 PCI performance...

Measured RX PCI performance: 3.355 Gbytes/sec
Measured RX PCI latency: 5.884 usec

Starting DEV0 channels...

Channel #1 started.
Channel #2 started.
Channel #3 started.
Channel #4 started.

Measuring the DEV1 PCI performance...

Measured TX PCI performance: 0.640 Gbytes/sec
Measured TX PCI latency: 7.223 nsec

Starting DEV1 channels...

Channel #1 started.
Channel #2 started.

Waiting for all channels to stop processing (interrupts disabled)...

WARNING: CTRL-C FROM THE KEYBOARD MAY CRASH THE COMPUTER!

Retrieving DEV0 temperature status...

INFO: FPGA die temperature is 42.11 degrees Celsius.
INFO: ADC proximity temperature is 35.00 degrees Celsius.
INFO: QDR proximity temperature is 39.00 degrees Celsius.
INFO: Shielded proximity temperature is 32.00 degrees Celsius.
INFO: Card center proximity temperature is 38.00 degrees Celsius.

Retrieving DEV0 power status...

INFO: Total power dissipation is 17.74 Watts.
INFO: Supply #1 summary: 3.36 Volts, 0.08 Amps, 0.28 Watts
INFO: Supply #2 summary: 12.09 Volts, 1.44 Amps, 17.46 Watts

Reviewing DEV0 channel status...

Saving captured data on all DEV0 receiver channels...

Writing channel #1 data buffer contents to file rx1data.txt.
Writing channel #1 DMA buffer contents to file dma1buf.txt.
Writing channel #2 data buffer contents to file rx2data.txt.
Writing channel #2 DMA buffer contents to file dma2buf.txt.
Writing channel #3 data buffer contents to file rx3data.txt.
Writing channel #3 DMA buffer contents to file dma3buf.txt.
Writing channel #4 data buffer contents to file rx4data.txt.
Writing channel #4 DMA buffer contents to file dma4buf.txt.

Retrieving DEV1 temperature status...

INFO: FPGA die temperature is 43.10 degrees Celsius.
INFO: ADC proximity temperature is 32.00 degrees Celsius.
INFO: QDR proximity temperature is 29.00 degrees Celsius.
INFO: Shielded proximity temperature is 31.00 degrees Celsius.
INFO: Card center proximity temperature is 30.00 degrees Celsius.

Retrieving DEV1 power status...

INFO: Total power dissipation is 9.48 Watts.
INFO: Supply #1 summary: 3.36 Volts, 0.30 Amps, 1.01 Watts
INFO: Supply #2 summary: 12.18 Volts, 0.13 Amps, 1.61 Watts
INFO: Supply #3 summary: 12.18 Volts, 0.56 Amps, 6.87 Watts

Reviewing DEV1 channel status...

Saving probe data on all DEV1 transmitter channels...

Writing the first 1024 DAC samples on channel #1 to file tx1probe.txt.
Writing the first 1024 DAC samples on channel #2 to file tx2probe.txt.

...all operations completed.