SigFPGA Model Number Options Decoder

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1.0 Introduction

The SigFPGA product family offers several analog interface options coupled to a common Kintex-7 based FPGA processing architecture. Each product is assigned a six-digit model number (Model XXX-YYY) that uniquely identifies the specific hardware features of that unit. The first three digits are the primary designator used to convey information about the structure of the analog front-end. The last three digits define the build options selected by a customer to tailor the product to a specific application.

1.1 Primary Designator

All of the SigFPGA primary model number designators are listed in Table 1-1. Each value defines the specific characteristics of the receiver and/or transmitter channels of the analog front-end. Please note that the actual sample rate is defined by the synthesizer build option and not necessarily the maximum rate supported by the channel.

Table 1-1 Primary Model Number Designators

Primary Designator	RX Channels	TX Channels	Maximum Sample Rate
371	2 / 16 bits	0	250 Msps
372	2 / 16 bits	2 / 16 bits	310 Msps
373	2 / 16 bits	0	310 Msps
376	2 / 12 bits	0	1.6 Gsps
377	4 / 16 bits	0	250 Msps
378	8 / 16 bits	0	125 Msps

1.2 Build Options

There are several build options available within each primary designator. These numbers are created as needed when a customer requests a configuration that has not previously been ordered. **Table** 1-2 lists all of the current model numbers in circulation throughout the customer base. This list continues to grow as new configurations are requested.

1.2.1 Synthesizer Frequency

The synthesizer frequency can be set to any value between the minimum and maximum sample rates supported by the front-end. Fixed frequency synthesizers are typically used to minimize phase noise, but programmable synthesizers are also available to cover a range of frequencies.

1.2.2 Form Factor

The SigFPGA products are available in three different form factors; PCIe, XMC, and CCXMC. Although these options are self-explanatory, it is worth noting that some PCIe products are actually XMC boards mounted to a PCIe/XMC carrier. They behave the same as a native PCIe product. Some PCIe products support either the traditional horizontal SMA (H-SMA) connectors through the face plate or vertical SMA (V-SMA) connectors across the top of the card for wiring internal to the chassis.

1.2.3 Analog Coupling

All of the SigFPGA products support AC coupling at the analog RX/TX interface and most also support DC coupling. The DC coupled option is only necessary when frequencies below a few hundred kilohertz are important.

1.2.4 Coaxial Inputs

Some of the SigFPGA products have individual coaxial clock and trigger inputs while others have a single connector that must be configured as one or the other.

The CLK/REF option accepts either a 10 MHz reference to phase lock the on-board frequency synthesizer, or an external sample clock to bypass the synthesizer.

The TRIG option accepts either an external trigger to control channel processing or a 1 PPS timing source to synchronize the on-board time of day clock. The coaxial trigger input can be terminated into 50 ohms or a high impedance (HI-Z) buffer.

1.2.5 FPGA Size/Speed

The SigFPGA product supports three different Kintex-7 size options; XC7K160T, XC7K325T, and XC7K410T. Each part is offered in either the -2 or -3 speed grade.

1.2.6 Configuration Flash Protection

The FPGA configuration flash memory can always be accessed through the GPIO connector using a Xilinx programming cable. The flash can also be programmed from the FPGA logic, but only if it is write enabled (WE). The write protect (WP) option is available to customers that want to eliminate this capability for security reasons.

1.2.7 SRAM

There are two QDR II+ SRAM chips connected to the FPGA for applications that require external high speed storage. This feature is not needed in many applications and there is both a cost and power savings if those chips are depopulated.

The initial release of SigFPGA products used a fixed 450 MHz oscillator to clock the SRAM. Later releases employed the Xilinx spread spectrum clock generator to reduce spurious interference.

1.2.8 GPIO Voltage

The GPIO connector is used to interface external digital signals to the FPGA. The electrical interface supports 3.3 V LVCMOS, 2.5 V LVCMOS, 1.8 V LVCMOS, or LVDS signaling standards.

1.2.9 USER Voltage

The USER connector is used to interface external digital signals to the FPGA. The electrical interface supports 3.3 V LVCMOS, 2.5 V LVCMOS, or LVDS signaling standards.

1.2.10 Configuration Flash

The configuration flash is used to store the FPGA bitstream. The specific device used on a build option is factory selected.

Table 1-2 Active Model Numbers

Model Number	Synthesizer Frequency (MHz)	PCIe (H-SMA)	PCIe (V-SMA)	CCXMC	XMC	AC RX Channels	DC RX Channels	AC TX Channels	DC TX Channels	Coax CLK/REF	Coax TRIG (50 Ω)	Coax TRIG (HI-Z)	XC7K160T-2	XC7K325T-2	XC7K325T-3	XC7K410T-2	XC7K410T-3	WE Flash	WP Flash	SRAM (450 MHz)	SRAM (Spread)	3.3V GPIO	3.3V USER	2.5V USER	MT28GU512 Flash	MT28GU256 Flash
371-001	250			X			2			X		X				X		X		X		X	X		X	
371-002	213.33				X	2				X	X					X		X				X		X	X	
371-100	250			X		2				X		X	X					X				X	X		X	
371-400	250	X				2				X	X					X		X			X	X	X		X	
372-003	200				X	2			2	X				X				X				X		X	X	
372-101	200			X		2			2	X					X			X				X	X			X
372-500	250	X				2		2		X				X				X				X		X	X	
372-501	310	X				2		2		X				X				X				X		X	X	
373-001	213.33				X	2				X	X		X					X				X	X		X	
373-100	310			X			2			X		X	X					X				X	X		X	
376-001	1333.33				X	2				X		X				X			X	X		X		X	X	
376-003	1333.33				X	2				X		X				X		X				X	X		X	
376-101	1333.33			X		2				X		X				X			X	X		X		X	X	
376-500	1333.33	X				2				X		X				X			X	X		X		X	X	
376-501	1333.33	X				2				X		X				X		X				X	X		X	
377-100	250			X		4						X		X				X				X	X		X	
377-403	250	X				4				X			X					X		X		X	X		X	
377-405	213.33		X			4				X							X	X		X		X	X		X	
378-001	125				X	8				X			X					X				X		X		X