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Clock Distribution System 006-005
1500 MHz Single RX Reference Manual

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1.0 Introduction

1.1 Contents and Structure

This manual describes the 006-005 Front-End clock distribution system. The focus of this manual is the electrical function of the clock system and key components.

The latest product documentation and software is available for download from the Red Rapids web site (www.redrapids.com) by following the Technical Support link.

1.2 Conventions

This manual uses the following conventions:

- Hexadecimal numbers are prefixed by "0x" (e.g. 0x00058C).

☞	Text in this format highlights useful or important information.

!	Text shown in this format is a warning. It describes a situation that could potentially damage your equipment. Please read each warning carefully.

The following are acronyms used in this manual.

- **CLK** Sample Clock
- **dB** Decibels
- **dBFS** Decibels Relative to Full Scale
- **dBm** Decibels Relative to One milliwatt
- **MHz** Megahertz
- **mV** millivolts
- **MSPS** Mega Samples per Second
- **PLL** Phase-Locked Loop
- **REF** Reference Clock
- **RF** Radio Frequency
- **SFDR** Spur Free Dynamic Range
- **SINAD** Signal-to-Noise and Distortion Ratio
- **SPI** Serial Peripheral Interface
- **SNR** Signal-to-Noise Ratio
- **TCXO** Temperature Compensated Crystal Oscillator
- **Vpp** Voltage, peak-to-peak

1.3 Revision History

Version	Date	Description
R00	4/08/2016	Initial release.

2.0 Description

Red Rapids' products feature an on-board precision clocking system that provides a coherent timing source for its analog front ends. As shown in Figure 2-1 the front end clock structure consists of a sample clock source and switch.

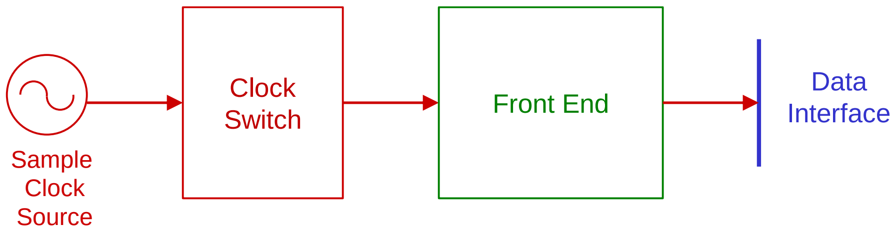


Figure 2-1 Front End Clocking Structure

The clock distribution system has three configurations implemented via connectivity as shown in Figure 2-2.

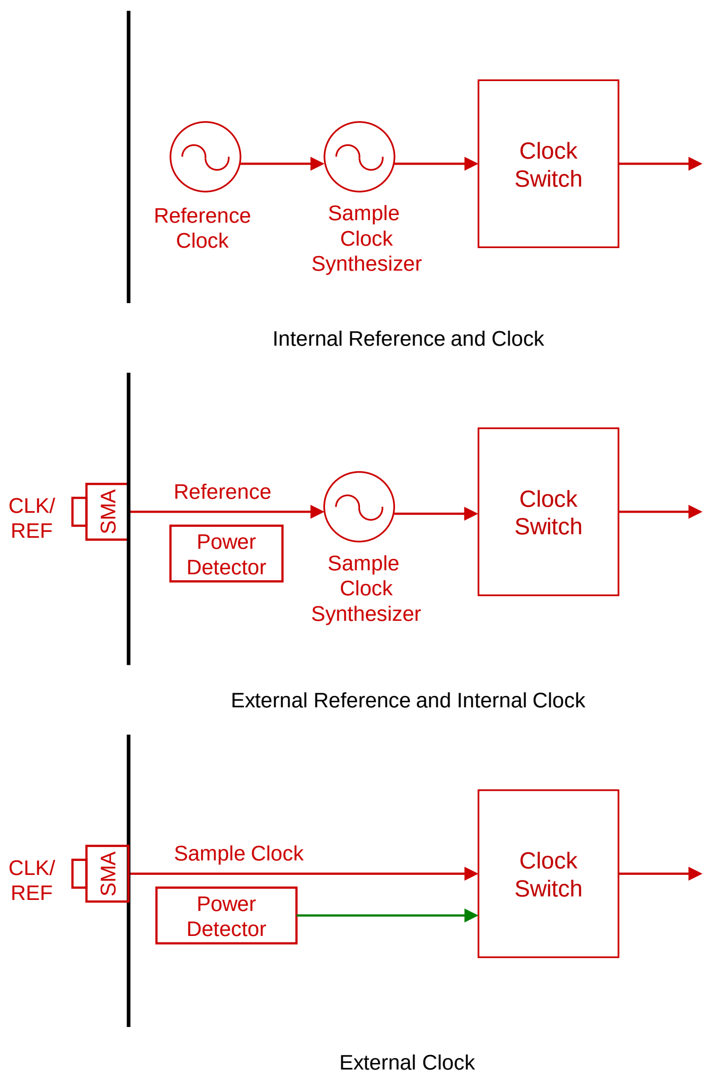


Figure 2-2 Sample Clock Structures

The three configurations are: internal reference and clock, external reference/internal clock and external clock. The external connections are made via a standard SMA-type coaxial connector and the clock switch is controlled by the external clock power detector. The external clock port is monitored by power detectors to provide status to the Control Interface and on-board LEDs. The following paragraphs detail the front-end clock distribution system.

2.1 Sample Clock Source

The front-end clock distribution system has two clock source options, a built-in internal phase-locked-loop synthesizer and an external user supplied sample clock as described in the following sections.

2.1.1 Internal Sample Clock

The internal sample clock consists of a low-noise oscillator in a phase-locked-loop (PLL) structure as shown in the diagram of Figure 2-3. The PLL is locked to a low frequency precision reference clock to provide long term stability. The PLL output is a low jitter high frequency sinewave used as the source for the front-end sample clock.

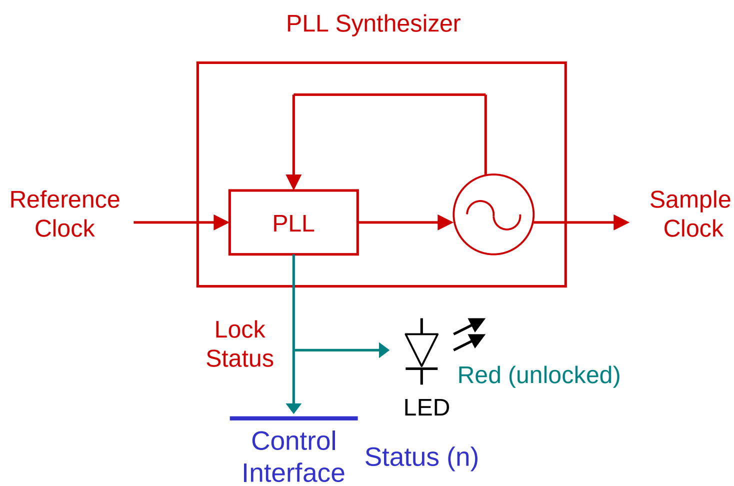
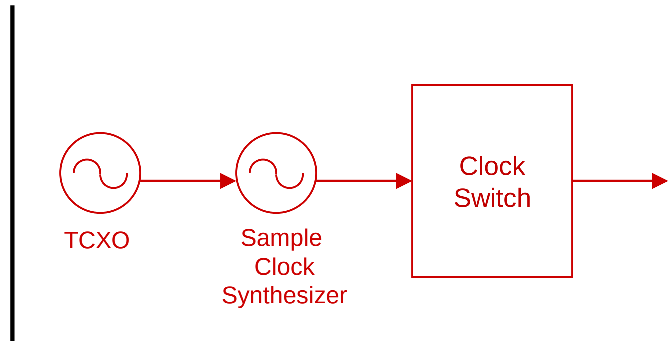


Figure 2-3 Internal Sample Clock Source

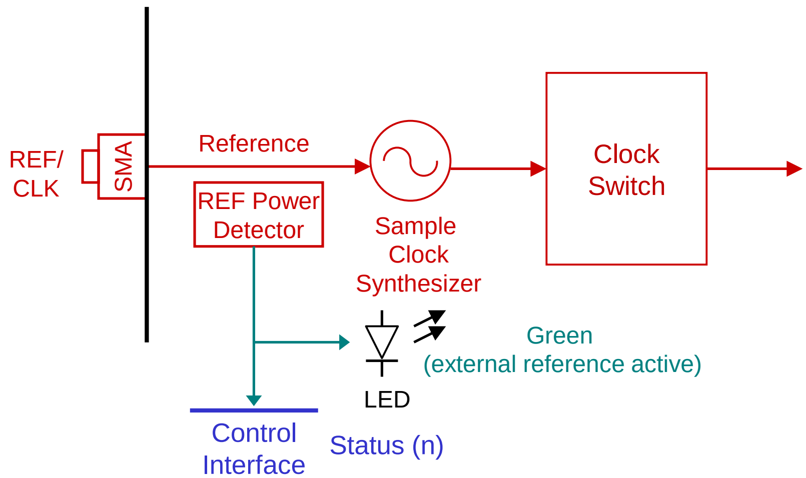
Synthesizer lock status is continually monitored and available to the user through the control interface. Additionally a red on-board LED will light should the synthesizer become unlocked. The synthesizer lock status passed to the Control Interface is not valid when an external sample clock is active as described in paragraph 2.1.2.

☞	Ignore the Control Interface Synthesizer lock status when an external sample clock is active.

There are two source options for the PLL reference clock, either the on-board TCXO or a user-provided reference supplied to the REF/CLK coaxial connector as shown in Figure 2-4. The following paragraphs describe the reference clock options.



Internal Reference and Clock



External Reference and Internal Clock

Figure 2-4 Internal Sample Clock Reference Options

2.1.1.1 On-board Reference Clock

The front-end clock distribution system features a built-in TCXO to round out a self-contained clocking solution. The input signal power on the REF/CLK SMA connector is constantly monitored to determine clock presence, if no external clock is detected the internal TCXO reference clock is activated.

The TCXO provides excellent long term stability for applications that do not require coherence to a system reference clock. Information on the built-in TCXO specifications can be found in the manufacturer's data sheet listed in section 5.0, performance data is shown in section 3.2 and a phase noise plot is shown in section 4.1.1.

2.1.1.2 External Reference Clock

An external reference clock connection is provided for users that require coherency to a system reference. The on-board frequency synthesizer can be phase locked to an external 10 MHz system reference to achieve system-wide phase coherence by simply connecting a source to the reference/clock SMA connector.

The input RF power level on the REF/CLK SMA is continuously monitored to detect the presence of an external source. If the power level exceeds an established operating threshold then the internal TCXO power is automatically turned off, the external reference is connected to the internal synthesizer and the external reference present status is passed to the control interface. An on-board green LED will illuminate when the external reference is active. Hysteresis is built into the detection circuit to prevent oscillation around the detection threshold.

Only a high quality low phase noise (< -145 dBc/Hz @ 10 kHz) source should be used as an external reference. External reference source harmonic content above 50 MHz exceeding a level of -10dBm will cause the external clock detector to trip and supply the wrong sample clock. Clock input level requirements can be found in section 3.1.

☞	Generally the synthesized output of an RF signal generator should not be used as a 10 MHz reference source due to high phase noise. Most generators feature a separate dedicated low phase noise 10 MHz reference output that should be used instead.

☞	Only a high quality low phase noise (< -145 dBc/Hz @ 10 kHz) source should be used as an external reference.

☞	The spectral power level of the external reference source above 50 MHz must be less than -10dBm.

2.1.2 External Sample Clock

The external sample clock mode connects the clock switch directly to the REF/CLK coaxial connector as shown in Figure 2-5. A detector continuously monitors the signal power on the REF/CLK port to determine the presence of an external clock. Once a signal is detected the on-board synthesizer is turned off, the clock switch is set to pass the external clock, an external clock present status is conveyed to the control interface and a yellow on-board LED illuminates indicating the presence of an external clock source.

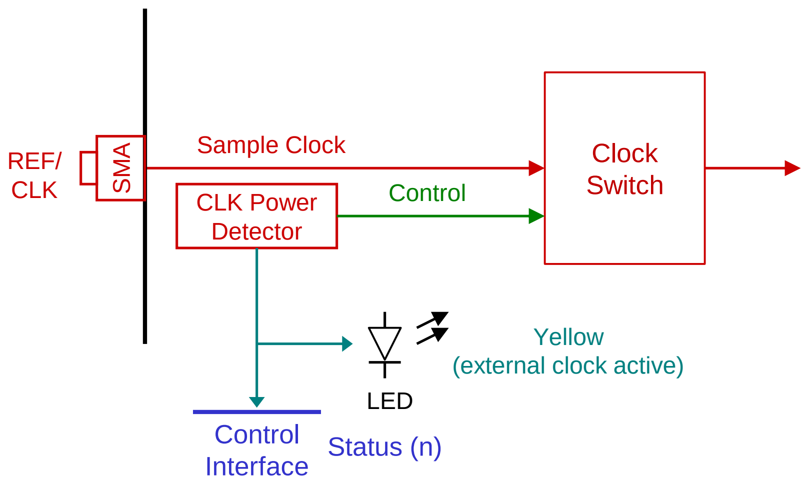


Figure 2-5 External Sample Clock Source

☞	The on-board synthesizer does not operate when an external sample clock is present.

An external sample clock signal is usually supplied by a high quality source that can provide good frequency stability (< +/- 2ppm) and low phase noise (<90 dBc/Hz @ 10 kHz, <1 ps rms jitter). Quality RF Test equipment may be used as a sample clock source as long as it meets the sample clock frequency and power requirements listed in section 3.1.

☞	The SNR of high frequency signals (Fin>100 MHz) can be improved by using an external sample clock with better phase noise than that of the internal synthesizer.

The user supplied external clock waveform may be sinusoidal or square as long as the phase noise/jitter characteristic is low. Sine wave inputs should operate at the high end of the permissible input power range to maximize the voltage slope into the ADC clock circuitry. Square wave inputs may be driven at a lower power level since they already have a steep voltage slope.

☞	The user supplied external sample clock may be sinusoidal or square in nature so long as it possesses a low phase noise/jitter characteristic.

2.2 Sample Clock Distribution

The analog front end relies on a coherent low noise distribution network to provide a sample clock to analog components and the front-end Data Interface as shown in Figure 2-6.

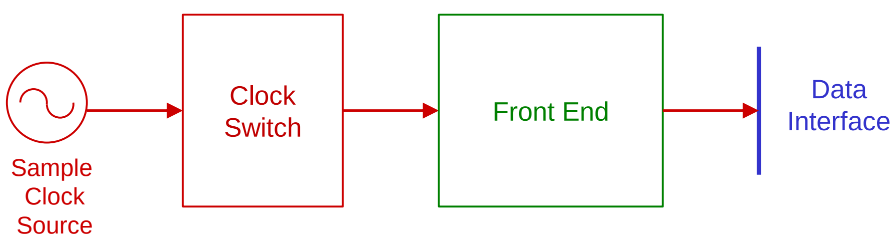


Figure 2-6 Clock Distribution Block Diagram

Clock distribution is performed using a single clock switch as shown in the diagram of Figure 2-7. The clock power detector automatically selects the external clock as a source when a clock is detected on the REF/CLK coaxial input. The front-end ADC provides a derivative of the sample clock in the form of a data clock to the Data Interface

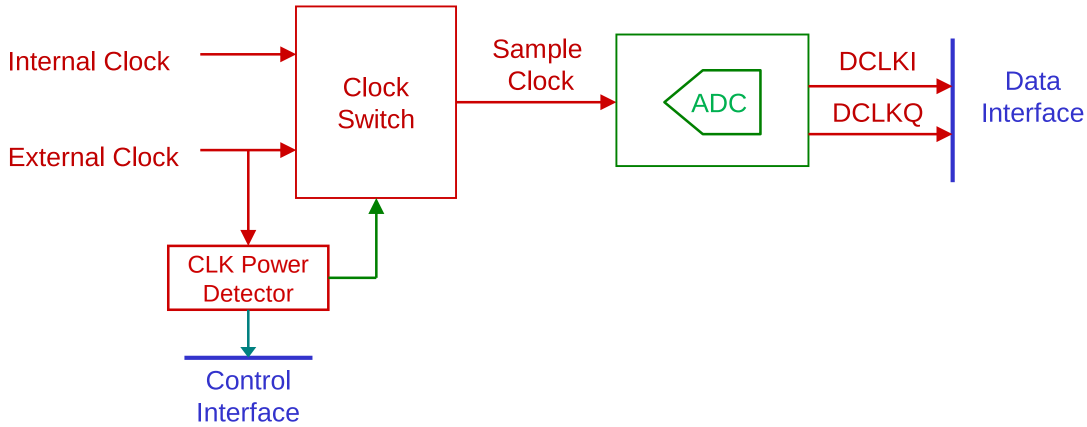


Figure 2-7 Clock Switch

3.0 Specifications

The following section lists the performance specifications of the Front End Clock Distribution System based on direct unit measurement unless otherwise noted. Measurements are listed as typical and represent the mean performance of a representative sample of units under laboratory conditions. Some variation in performance will occur based on build variation, external system performance and environment. See key component device data sheets in section 0 for more insight on performance variation.

3.1 External Reference and Sample Clock Specifications

Parameter	Min	Typ	Max	Unit
External Reference (REF)				
Input Impedance		50		Ohms
Input Voltage (50 Ohms)	1.5		3.0	Vpp
Input Power (50 Ohms)	+7		+13.5	dBm
Frequency	10		10	MHz
External Clock Input (CLK)				
Input Impedance		50		Ohms
Input Voltage (50 Ohms)	1	2.0	2.0	Vpp
Input Power [1] (50 Ohms)	+4	+10	+10	dBm
Frequency	500		750	MHz

Notes: [1] See external clock discussion on square vs. sine input.

3.2 Internal Reference and Sample Clock Performance

☞ Performance may vary depending on the quality of the power supply and EMI environment of the host.

Parameter	Min	Typ	Max	Unit
Internal Sample Clock				
Frequency (default)		750		MHz
Reference Spurs			75	dBc
Phase Noise				
1 kHz offset		-90	-85	dBc/Hz
10 kHz offset		-95	-90	dBc/Hz
100 kHz offset		-115	-110	dBc/Hz
Internal Reference				
Frequency (default)		10		MHz
Stability	-1.0		+1.0	ppm
Phase Noise				
1 kHz offset		-125		dBc/Hz
10 kHz offset		-145		dBc/Hz
100 kHz offset		-148		dBc/Hz

3.3 Absolute Maximums

Stresses above those listed in Table 3-1 may cause damage to the unit. The operation of the unit at these or any other conditions outside of those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may degrade unit reliability.

Table 3-1 Absolute Maximum Specifications

Parameter	Min	Typ	Max	Unit
Reference Clock Input (50 Ohms)				
DC Level	-10		10	V
AC Swing			3.6	Vpp
AC Power			+15.1	dBm
Sample Clock Input (50 Ohms)				
DC Level	-10		10	V
AC Swing			4	Vpp
AC Power			+16	dBm

!	Exposure to absolute maximum conditions for extended periods may degrade unit reliability.

4.0 Internal Clock Phase Noise Plots

The Front-End Clock Distribution System contains two internal clock sources, a fixed reference clock and a PLL synthesizer. The following sections provide plots of the typical phase noise response for the reference and synthesizer clock sources.

4.1.1 Internal Reference Phase Noise Response

Figure 4-1 shows the typical phase noise response for the internal reference. Note that the plot in Figure 4-1 is for a 12.8 MHz reference, the reference used in the Front-End Clock Distribution system is 10 MHz. The relative phase noise performance is the same.

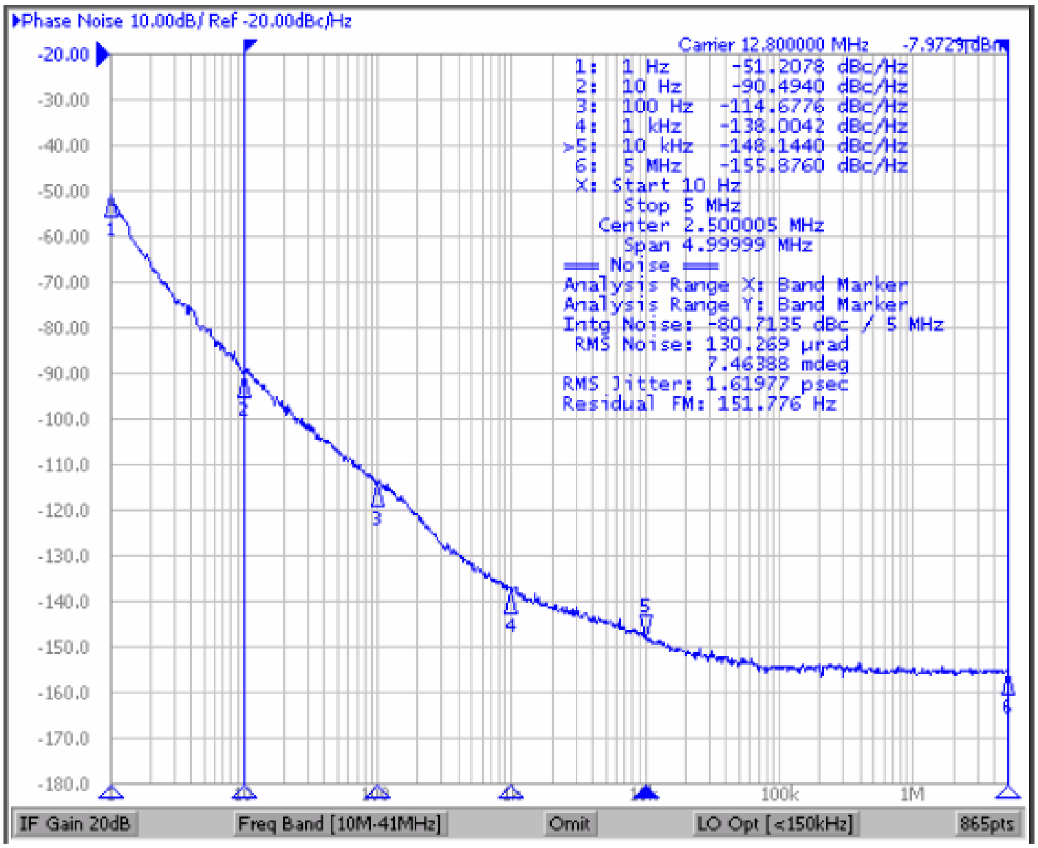


Figure 4-1 Phase Noise Response Plot for Internal Reference

4.1.2 Synthesizer Phase Noise Response

Figure 4-2 shows the typical phase noise response for the PLL synthesizer. Note that the plot in Figure 4-1 is for a 213.33 MHz synthesizer, the standard synthesizer for this system is 750 MHz. The relative phase noise performance is the same.

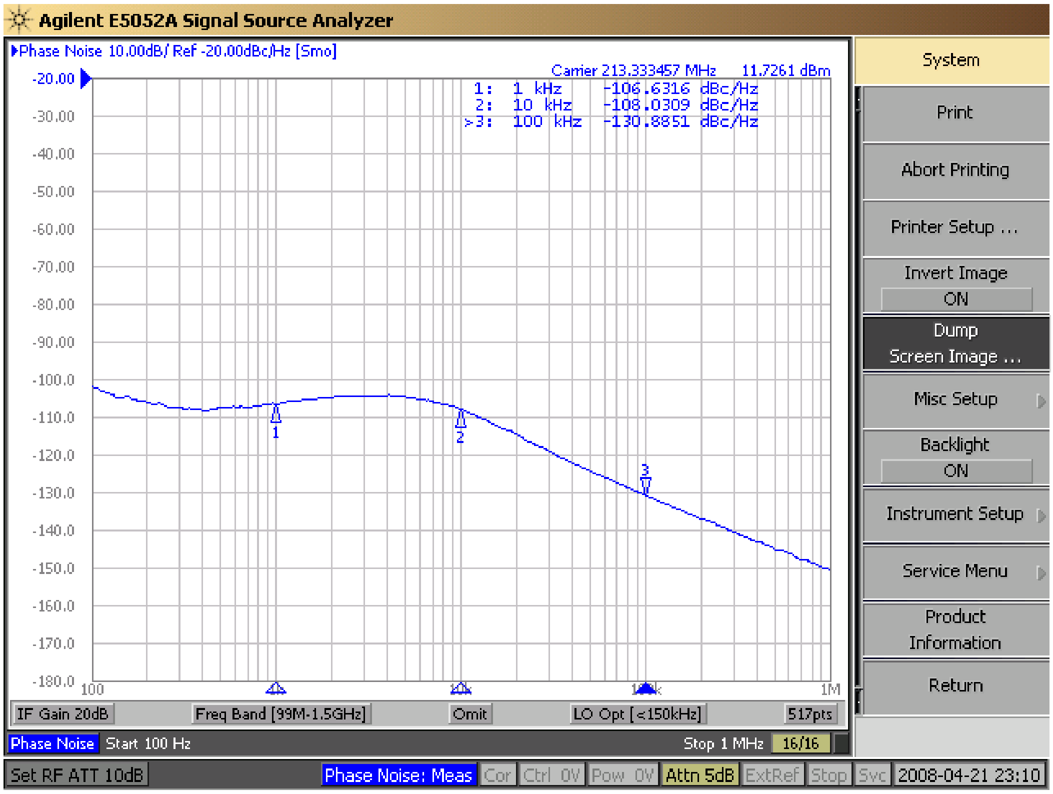


Figure 4-2 Phase Noise Response Plot for Synthesizer

5.0 Key Components

Key hardware components for the Receiver are listed in Table 5-1. Device datasheets can be downloaded from vendor websites for more information.

Table 5-1 Key Hardware Components

Component	Part Number	Vendor	Comments
TCXO	TV105AGBDT10M00	Bliley	10MHz TCXO 1.0ppm

6.0 Technical Support

Please feel free to contact us if you have a technical question about or problem with our product. We understand that our customers have tight deadlines and time is of the essence in development and production cycles. We will make every effort to resolve problems as quickly as possible.

Web: www.redrapids.com

Email: support@redrapids.com

Phone: 972-671-9570

Fax: 972-671-9572

Please include the following information with your correspondence:

Contact Information

Product Model

Host Card or System (PC, PCI Carrier, Single Board Computer)

Operating System

Problem Description