PCIe D-Sub Digital I/O

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1.0 Introduction

The FPGA based DSP accelerator products in PCIe format include a D-Subminiature (D-Sub) connector on the rear edge of the card for user-defined I/O. This manual describes the connectivity and electrical characteristics of the 68-pin D-Sub connector interface.

It is important to note that there are two types of PCIe products offered by Red Rapids. The first is an XMC module mounted to a PCIe/XMC carrier that consists of two circuit boards sandwiched together (Type A). The first is native PCIe hardware consisting of a single circuit board (Type B). The pinout is not the same for the two board types.

The latest product documentation and software is available for download from the Red Rapids website (www.redrapids.com).

1.1 Conventions

This manual uses the following conventions:

☞	Text in this format highlights useful or important information.

!	Text shown in this format is a warning. It describes a situation that could potentially damage your equipment. Please read each warning carefully.

The following are some of the acronyms used in this manual.

- **D-Sub** Type D Subminiature Connector
- **FPGA** Field Programmable Gate Array
- **LVCMOS** Low Voltage Complementary Metal Oxide Semiconductor
- **LVDS** Low Voltage Differential Signaling
- **PCIe** Peripheral Component Interconnect Express
- **SCSI** Small Computer System Interface
- **XDC** Xilinx Design Constraints

1.2 Revision History

Version	Date	Description
R00	1/15/2016	Initial release.

2.0 D-Sub Connector

The circuit board mounted 68-pin D-Sub connector, shown in Figure 2-1, provides a space efficient solution for external digital I/O. Mounting posts securely attach the connector to the PWB to reduce strain on the solder tails.

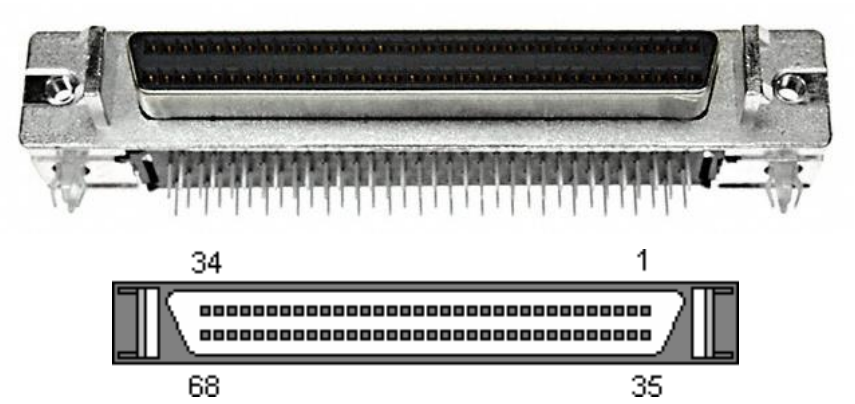

Figure 2-1 68-pin D-Sub Receptacle

The 68-pin D-Sub connector is commonly used in commercial SCSI peripherals, so there a wide range of existing connector and cable hardware readily available from multiple vendors. Figure 2-2 shows one example of a TE Connectivity cable plug (PN 5749621-7) and backshell (PN 5749195-2) that mates to the receptacle with two spring loaded latches.

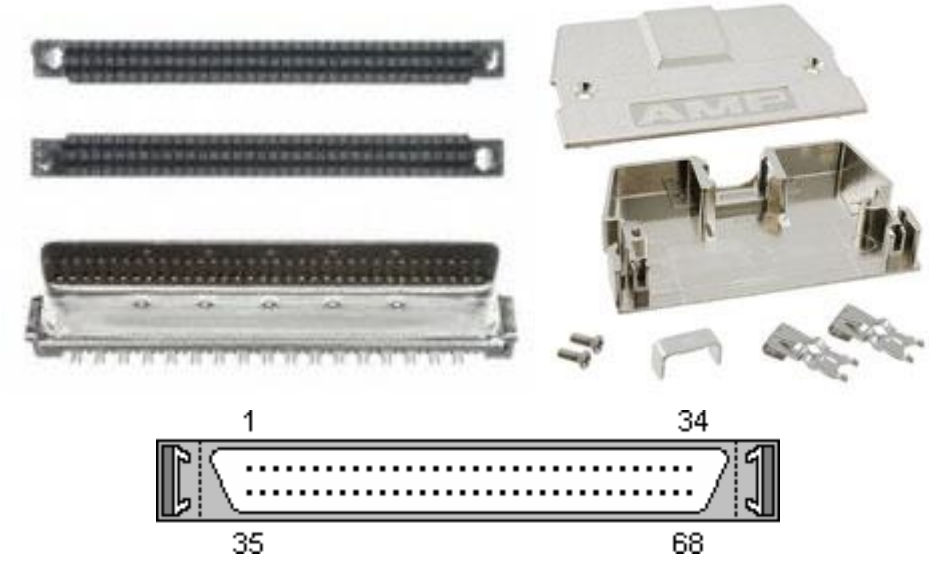

Figure 2-2 68-pin D-Sub Cable Plug

3.0 Connector Pinout

The D-Sub connector is wired to two different FPGA I/O banks as shown in Figure 3-1. The first fifty pins are wired directly to Bank 16, which can be powered by 2.5 V or 3.3 V as a build option. The remaining pins are wired to Bank 15 through voltage translators that can also be powered by either 2.5 V or 3.3 V. The translators shield the 1.8 V I/O in Bank 15 from the user-defined pins.

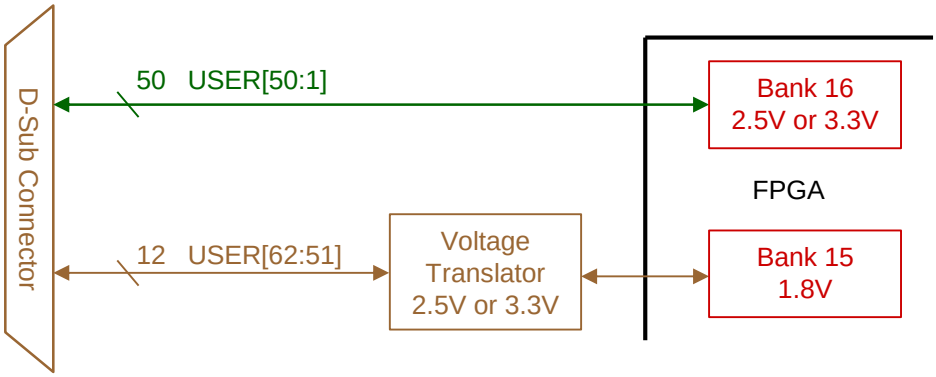

Figure 3-1 D-Sub Connector Wiring

The mapping of D-Sub connector pins to FPGA pins is product dependent. The following subsections list the pinout based on design type as defined below:

- Type A: D-Sub connectors attached to a PCIe/XMC carrier.
- Type B: D-Sub connectors attached to native PCIe hadware.

Some products include a silkscreen note near the connector to indicate the type.

3.1 Type A Pinout

The Type A pinout applies to D-Sub connectors attached to a PCIe/XMC carrier. The pin assignments for the USER interface to the D-Sub connector are listed in Table 3-1. The FPGA pin assignments are also supplied in a Xilinx Design Constraints (XDC) file that is distributed with the product FPGA development kit. The XMC variant of the XDC file should be used for Type A designs.

Table 3-1 Type A D-Sub User Defined Connector Pinout

Name	FPGA Pin	D-Sub Pin	D-Sub Pin	FPGA Pin	Name
USER1(N1) (1)	A15	1	35	B15	USER3(P1) (1)
USER2(N2) (1)	A14	2	36	B14	USER4(P2) (1)
USER5(N3) (1)	A12	3	37	A13	USER7(P3) (1)
USER6(N4) (1)	B11	4	38	B12	USER8(P4) (1)
USER9(N5) (1)	A10	5	39	B10	USER11(P5) (1)
USER10(N6) (1)	A8	6	40	A9	USER12(P6) (1)
USER13(N7) (1)	C13	7	41	C14	USER15(P7) (1)
USER14(N8) (1)	C11	8	42	C12	USER16(P8) (1)
USER17(N9) (1)	B9	9	43	C9	USER19(P9) (1)
GND or 3.3 V		10	44		GND
USER18(N10) (1)	D13	11	45	D14	USER20(P10) (1)
USER21(N11) (1)	E12	12	46	E13	USER23(P11) (1)
USER22(N12) (1)	D11	13	47	E11	USER24(P12) (1)
USER25(N13) (1)	D10	14	48	E10	USER27(P13) (1)
USER26(N14) (1)	D8	15	49	D9	USER28(P14) (1)
USER29(N15) (1)	F13	16	50	F14	USER31(P15) (1)
USER30(N16) (1)	F12	17	51	G12	USER32(P16) (1)
USER33(N17) (1)	F10	18	52	G11	USER35(P17) (1)
USER34(N18) (1)	G9	19	53	G10	USER36(P18) (1)
USER37(N19) (1)	F8	20	54	F9	USER39(P19) (1)
USER38(N20) (1)	G14	21	55	H14	USER40(P20) (1)
USER41(N21) (1)	H13	22	56	J13	USER43(P21) (1)
USER42(N22) (1)	H11	23	57	H12	USER44(P22) (1)
USER45(N23) (1)	J10	24	58	J11	USER47(P23) (1)
USER46(N24) (1)	H8	25	59	H9	USER48(P24) (1)
GND or 12 V		26	60		GND
USER49(1,2)	J14	27	61	C16	USER51(2,3,4)
USER50(1,2)	J8	28	62	B16	USER52(2,3,4)
USER53(2,3,4)	D15	29	63	E15	USER55(2,3,5)
USER54(2,3,4)	D16	30	64	E16	USER56(2,3,5)
USER57(2,3,5)	G17	31	65	G15	USER59(2,3,6)
USER58(2,3,5)	F18	32	66	F15	USER60(2,3,6)
USER61(2,3,6)	H16	33	67		Reserved
USER62(2,3,6)	G16	34	68		Reserved

Notes: (1) Pin has a direct connection to the FPGA (VCCO = 2.5 V or 3.3 V as a build option).
(2) Pin cannot be used in an LVDS differential pair.
(3) Pin connects to the FPGA through a bidirectional translator.
(4) Pin has a direct connection to the FPGA (VCCO = 2.5 V or 3.3 V as a build option).
(5,6,7) Pins in each group can be set to 2.5 V or 3.3 V LVCMOS as a build option.

3.2 Type B Pinout

The Type B pinout applies to D-Sub connectors attached to native PCIe hardware. The pin assignments for the USER interface to the D-Sub connector are listed in Table 3-2. The FPGA pin assignments are also supplied in a Xilinx Design Constraints (XDC) file that is distributed with the product FPGA development kit. The PCIe variant of the XDC file should be used for Type B designs.

Table 3-2 Type B D-Sub User Defined Connector Pinout

Name	FPGA Pin	D-Sub Pin	D-Sub Pin	FPGA Pin	Name
USER1(N1) (1)	H11	1	35	H12	USER2(P1) (1)
USER3(N2) (1)	J10	2	36	J11	USER4(P2) (1)
GND		3	37	G17	USER57(2,3,5)
USER5(N3) (1)	H13	4	38	J13	USER6(P3) (1)
USER7(N4) (1)	H8	5	39	H9	USER8(P4) (1)
USER9(N5) (1)	G14	6	40	H14	USER10(P5) (1)
USER11(N6) (1)	F10	7	41	G11	USER12(P6) (1)
USER13(N7) (1)	G9	8	42	G10	USER14(P7) (1)
USER58(2,3,5)	F18	9	43		GND
USER15(M9) (1)	F8	10	44	F9	USER16(P8) (1)
USER17(N9) (1)	F12	11	45	G12	USER18(P9) (1)
USER19(N10) (1)	F13	12	46	F14	USER20(P10) (1)
USER21(N11) (1)	D11	13	47	E11	USER22(P11) (1)
USER23(N12) (1)	D8	14	48	D9	USER24(P12) (1)
GND		15	49	G15	USER59 (2,3,6)
USER25(N13) (1)	D10	16	50	E10	USER26(P13) (1)
USER27(N14) (1)	E12	17	51	E13	USER28(P14) (1)
USER29(N15) (1)	D13	18	52	D14	USER30(P15) (1)
USER31(N16) (1)	C11	19	53	C12	USER32(P16) (1)
USER60 (2,3,6)	F15	20	54		GND
USER33(N17) (1)	B9	21	55	C9	USER34(P17) (1)
USER35(N18) (1)	A10	22	56	B10	USER36(P18) (1)
USER37(N19) (1)	A8	23	57	A9	USER38(P19) (1)
USER39(N20) (1)	C13	24	58	C14	USER40(P20) (1)
USER41(N21) (1)	B11	25	59	B12	USER42(P21) (1)
GND		26	60	H16	USER61(2,3,6)
USER43(N22) (1)	A12	27	61	A13	USER44(P22) (1)
USER45(N23) (1)	A14	28	62	B14	USER46(P23) (1)
USER47(N24) (1)	A15	29	63	B15	USER48(P24) (1)
USER49(1,2)	J14	30	64	J8	USER50(1,2)
USER51(2,3,4)	C16	31	65	B16	USER52(2,3,4)
USER62(2,3,6)	G16	32	66		GND
USER53(2,3,4)	D15	33	67	D16	USER54(2,3,4)
USER55(2,3,5)	E15	34	68	E16	USER56(2,3,5)

Notes: (1) Pin has a direct connection to the FPGA (VCCO = 2.5 V or 3.3 V as a build option).
(2) Pin cannot be used in an LVDS differential pair.
(3) Pin connects to the FPGA through a bidirectional translator.
(4) Pin has a direct connection to the FPGA (VCCO = 2.5 V or 3.3 V as a build option).
(5,6,7) Pins in each group can be set to 2.5 V or 3.3 V LVCMOS as a build option.

4.0 Electrical Characteristics

The electrical characteristics of USER[50:1] will be determined by the IOB selected for each FPGA pin. The available I/O standards are limited by the power option selected for Bank 16 (2.5 V or 3.3 V). Consult the Kintex-7 FPGA Data Sheet from Xilinx for further details.

The USER[62:51] signals are connected to the FPGA through bidirectional voltage translators (Fairchild PN FXL4TD245). The LVCMOS electrical characteristics presented at the connector are listed in Table 4-1 for both the 2.5 V and 3.3 V build options.

Table 4-1 USER[62:51] Electrical Characteristics

Symbol	Description	2.5 V		3.3 V	
		MIN	MAX	MIN	MAX
V_{IH}	High Level Input Voltage	1.6 V	N/A	2.0 V	N/A
V_{IL}	Low Level Input Voltage	N/A	0.7 V	N/A	0.8 V
I_{OL}, I_{OH}	Output Current	N/A	±18 mA	N/A	±24 mA
V_{OH}	I_{OH} = MAX	1.7 V	N/A	2.2 V	N/A
V_{OL}	I_{OL} = MAX	N/A	0.6 V	N/A	0.55 V
t_{IPLH}, t_{IPHL}	Input Propagation Delay	0.5 ns	5.6 ns	0.5 ns	5.4 ns
t_{OPLH}, t_{OPHL}	Output Propagation Delay	0.5 ns	4.5 ns	0.3 ns	4.0 ns
C_{IO}	Input/Output Capacitance	5.0 pF (typical)			