# XMC P4 Digital I/O

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# 1.0 Introduction

The FPGA based DSP accelerator products in XMC format include the P4 user-defined I/O connector from the legacy IEEE 1386.1 (PMC) specification. This connector provides an auxiliary digital communication path to the host. This manual describes the connectivity and electrical characteristics of the 64-pin IEEE 1386 connector interface.

The latest product documentation and software is available for download from the Red Rapids website (www.redrapids.com).

## 1.1 Conventions

This manual uses the following conventions:

| | |
|---|---|
| ☞ | Text in this format highlights useful or important information. |

| | |
|---|---|
| **!** | Text shown in this format is a warning. It describes a situation that could potentially damage your equipment. Please read each warning carefully. |

The following are some of the acronyms used in this manual.

- **CMC** Common Mezzanine Card
- **FPGA** Field Programmable Gate Array
- **IEEE** Institute of Electrical and Electronics Engineers
- **LVCMOS** Low Voltage Complementary Metal Oxide Semiconductor
- **LVDS** Low Voltage Differential Signaling
- **PCI** Peripheral Component Interconnect
- **PMC** PCI Mezzanine Card
- **XDC** Xilinx Design Constraints
- **XMC** Express Mezzanine Card

## 1.2 Revision History

| Version | Date | Description |
|---|---|---|
| R00 | 1/15/2016 | Initial release. |
| | | |

## 2.0 IEEE 1386 Connector

The circuit board mounted 64-pin IEEE 1386 connector, shown in Figure 2-1, provides the primary digital interface for the Common Mezzanine Card (CMC) form factor. Four of the connectors are available on a single width CMC. The same connector was carried forward to the PMC specification, which assigned PCI bus signals to three of the connectors and left the fourth (P4) for user-defined I/O. The XMC specification is backward compatible with the PMC connector placement, but only the P4 connector is supported on Red Rapids XMC products.

**Figure 2-1 64-pin IEEE 1386 Connector**

The 64-pin plug on the XMC mates with a companion 64-pin receptacle on the host. The routing of P4 signal connections on the host is vendor specific. Please consult documentation supplied with the host hardware for further information.

## 3.0 Connector Pinout

The IEEE 1386 connector is wired to two different FPGA I/O banks as shown in Figure 3-1. The first fifty pins are wired directly to Bank 16, which can be powered by 2.5 V or 3.3 V as a build option. The remaining pins are wired to Bank 15 through voltage translators that can also be powered by either 2.5 V or 3.3 V. The translators shield the 1.8 V I/O in Bank 15 from the user-defined pins.

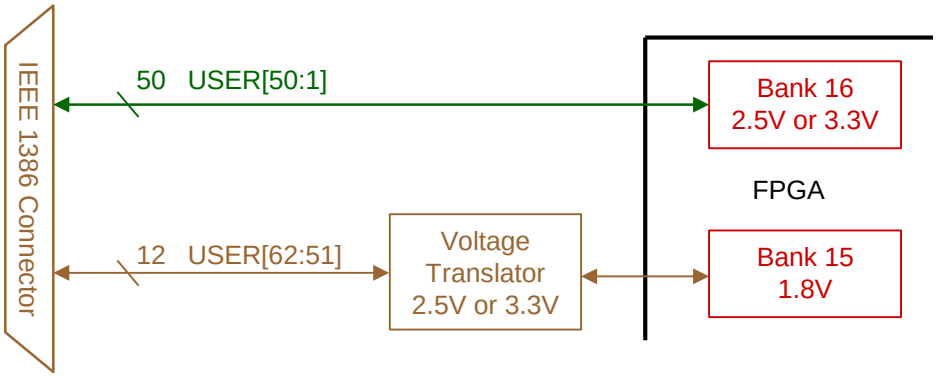


**Figure 3-1 IEEE 1386 Connector Wiring**

The pin assignments for the USER interface to the IEEE 1386 connector are listed in Table 3-1. The FPGA pin assignments are also supplied in a Xilinx Design Constraints (XDC) file that is distributed with the product FPGA development kit.

**Table 3-1 XMC P4 User Defined Connector Pinout**

| Name | FPGA Pin | P4 Pin | P4 Pin | FPGA Pin | Name |
|---|---|---|---|---|---|
| USER1(N1) (1) | A15 | 1 | 2 | A14 | USER2(N2) (1) |
| USER3(P1) (1) | B15 | 3 | 4 | B14 | USER4(P2) (1) |
| USER5(N3) (1) | A12 | 5 | 6 | B11 | USER6(N4) (1) |
| USER7(P3) (1) | A13 | 7 | 8 | B12 | USER8(P4) (1) |
| USER9(N5) (1) | A10 | 9 | 10 | A8 | USER10(N6) (1) |
| USER11(P5) (1) | B10 | 11 | 12 | A9 | USER12(P6) (1) |
| USER13(N7) (1) | C13 | 13 | 14 | C11 | USER14(N8) (1) |
| USER15(P7) (1) | C14 | 15 | 16 | C12 | USER16(P8) (1) |
| USER17(N9) (1) | B9 | 17 | 18 | D13 | USER18(N10) (1) |
| USER19(P9) (1) | C9 | 19 | 20 | D14 | USER20(P10) (1) |
| USER21(N11) (1) | E12 | 21 | 22 | D11 | USER22(N12) (1) |
| USER23(P11) (1) | E13 | 23 | 24 | E11 | USER24(P12) (1) |
| USER25(N13) (1) | D10 | 25 | 26 | D8 | USER26(N14) (1) |
| USER27(P13) (1) | E10 | 27 | 28 | D9 | USER28(P14) (1) |
| USER29(N15) (1) | F13 | 29 | 30 | F12 | USER30(N16) (1) |
| USER31(P15) (1) | F14 | 31 | 32 | G12 | USER32(P16) (1) |
| USER33(N17) (1) | F10 | 33 | 34 | G9 | USER34(N18) (1) |
| USER35(P17) (1) | G11 | 35 | 36 | G10 | USER36(P18) (1) |
| USER37(N19) (1) | F8 | 37 | 38 | G14 | USER38(N20) (1) |
| USER39(P19) (1) | F9 | 39 | 40 | H14 | USER40(P20) (1) |
| USER41(N21) (1) | H13 | 41 | 42 | H11 | USER42(N22) (1) |
| USER43(P21) (1) | J13 | 43 | 44 | H12 | USER44(P22) (1) |
| USER45(N23) (1) | J10 | 45 | 46 | H8 | USER46(N24) (1) |
| USER47(P23) (1) | J11 | 47 | 48 | H9 | USER48(P24) (1) |
| USER49(1,2) | J14 | 49 | 50 | J8 | USER50(1,2) |
| USER51(2,3,4) | C16 | 51 | 52 | B16 | USER52(2,3,4) |
| USER53(2,3,4) | D15 | 53 | 54 | D16 | USER54(2,3,4) |
| USER55(2,3,5) | E15 | 55 | 56 | E16 | USER56(2,3,5) |
| USER57(2,3,5) | G17 | 57 | 58 | F18 | USER58(2,3,5) |
| USER59(2,3,6) | G15 | 59 | 60 | F15 | USER60(2,3,6) |
| USER61(2,3,6) | H16 | 61 | 62 | G16 | USER62(2,3,6) |
| NC | | 63 | 64 | | NC |

Notes:

(1) Pin has a direct connection to the FPGA (VCCO = 2.5 V or 3.3 V as a build option).
(2) Pin cannot be used in an LVDS differential pair.
(3) Pin connects to the FPGA through a bidirectional translator.
(4) Pin group can be set to 2.5 V or 3.3 V LVCMOS as a build option.
(5) Pin group can be set to 2.5 V or 3.3 V LVCMOS as a build option.
(6) Pin group can be set to 2.5 V or 3.3 V LVCMOS as a build option.

# 4.0 Electrical Characteristics

The electrical characteristics of USER[50:1] will be determined by the IOB selected for each FPGA pin. The available I/O standards are limited by the power option selected for Bank 16 (2.5 V or 3.3 V). Consult the Kintex-7 FPGA Data Sheet from Xilinx for further details.

The USER[62:51] signals are connected to the FPGA through bidirectional voltage translators (Fairchild PN FXL4TD245). The LVCMOS electrical characteristics presented at the connector are listed in Table 4-1 for both the 2.5 V and 3.3 V build options.

**Table 4-1 USER[62:51] Electrical Characteristics**

| Symbol | Description | 2.5 V | | 3.3 V | |
|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX |
| $V_{IH}$ | High Level Input Voltage | 1.6 V | N/A | 2.0 V | N/A |
| $V_{IL}$ | Low Level Input Voltage | N/A | 0.7 V | N/A | 0.8 V |
| $I_{OL}$, $I_{OH}$ | Output Current | N/A | ±18 mA | N/A | ±24 mA |
| $V_{OH}$ | $I_{OH}$ = MAX | 1.7 V | N/A | 2.2 V | N/A |
| $V_{OL}$ | $I_{OL}$ = MAX | N/A | 0.6 V | N/A | 0.55 V |
| $t_{IPLH}$, $t_{IPHL}$ | Input Propagation Delay | 0.5 ns | 5.6 ns | 0.5 ns | 5.4 ns |
| $t_{OPLH}$, $t_{OPHL}$ | Output Propagation Delay | 0.5 ns | 4.5 ns | 0.3 ns | 4.0 ns |
| $C_{IO}$ | Input/Output Capacitance | 5.0 pF (typical) | | | |