Front Panel Digital I/O and Indicators

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Table of Contents

List of Figures

List of Tables

1.0 Introduction

The FPGA based DSP accelerator products include front panel digital I/O connectors to facilitate communication with external hardware. These connectors typically carry a JTAG bus, general purpose I/O (GPIO) signals, and triggers to the FPGA. This manual describes the connectivity and electrical characteristics of the 15-pin Nano-D connector interface and the optional coax trigger input.

There are two front panel LED indicators available to the FPGA application logic. This manual describes the characteristics of those indicators.

The latest product documentation and software is available for download from the Red Rapids website (www.redrapids.com).

1.1 Conventions

This manual uses the following conventions:

☞	Text in this format highlights useful or important information.

!	Text shown in this format is a warning. It describes a situation that could potentially damage your equipment. Please read each warning carefully.

The following are some of the acronyms used in this manual.

- **AWG** American Wire Gauge
- **FPGA** Field Programmable Gate Array
- **GPIO** General Purpose I/O
- **IEEE** Institute of Electrical and Electronics Engineers
- **JTAG** Joint Test Action Group
- **LED** Light Emitting Diode

1.2 Revision History

Version	Date	Description
R01	1/15/2016	Added SMA trigger input and LED indicators.
R00	3/7/2014	Initial release.

2.0 Nano-D Connector

The circuit board mounted 15-pin Nano-D connector, shown in Figure 2-1, provides a space efficient solution for external digital I/O. Two screws securely attach the connector to the PWB to eliminate strain on the solder joints. The Nano-D connector is labeled GPIO on products that include a bezel or face plate.

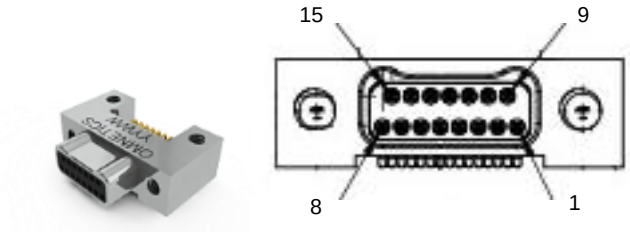
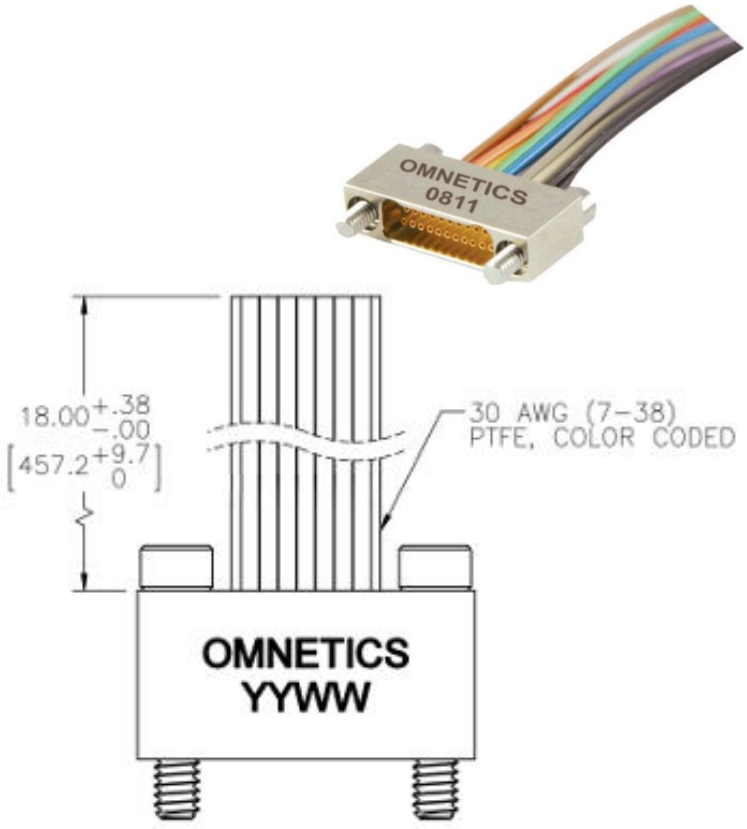


Figure 2-1 15-pin Nano-D Connector

An 18 inch Nano-D pigtail connector mates to the circuit board mounted connector. The connectors are secured using two hex head retention screws. The 30 AWG Teflon coated wires are color coded as shown in Figure 2-2. The pigtail connector assembly is available from Red Rapids or directly from Omnetics (PN A29000-115).



SOCKET #	COLOR
1, 11	BLACK
2, 12	BROWN
3, 13	RED
4, 14	ORANGE
5, 15	YELLOW
6	GREEN
7	BLUE
8	VIOLET
9	GRAY
10	WHITE

Figure 2-2 15-pin Nano-D Pigtail

2.1 Nano-D Pinout

The Nano-D connector supports three different FPGA functions as shown in Figure 2-3. Five pins are allocated to the JTAG programming interface, seven pins are allocated to the

GPIO function, and one pin is assigned to a 50 ohm terminated trigger. The remaining pins are assigned to power and ground.

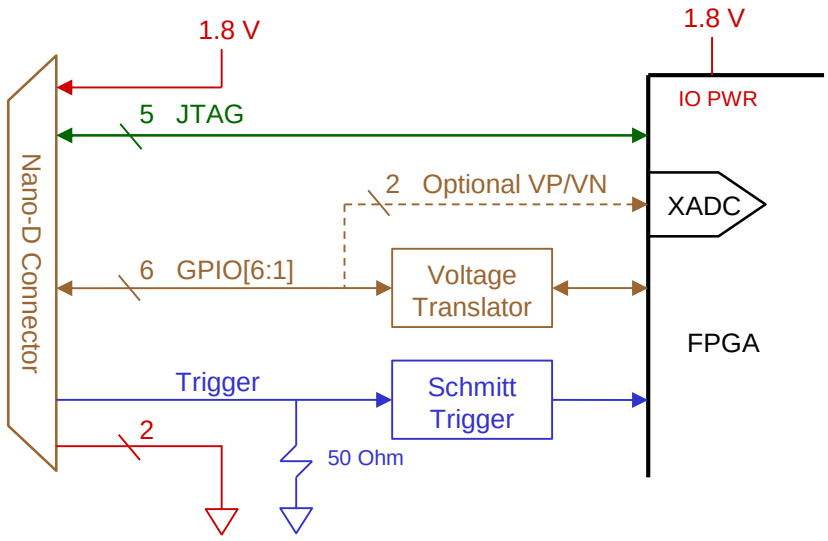


Figure 2-3 Nano-D Connector Wiring

Table 2-1 lists the signal assignments for all fifteen Nano-D connector pins. The FPGA pin assignments are also supplied in a Xilinx Design Constraints (XDC) file that is distributed with the product FPGA development kit.

Table 2-1 Nano-D Pin Assignments

Nano-D Pin	FPGA Pin	Signal Type	Signal Name
1	D23 or P11	Bidirectional or Analog Input	GPIO #1 or XADC_VN
2	D24 or N12	Bidirectional or Analog Input	GPIO #2 or XADC_VP
3	E25	Bidirectional	GPIO #3
4	D25	Bidirectional	GPIO #4
5	F22	Bidirectional	GPIO #5
6	E23	Bidirectional	GPIO #6
7	F24	Input	Trigger
8	N/A	Power	GND
9	N/A	Power	GND
10	N8	Input	TMS
11	L8	Input	TCK
12	R7	Output	TDO
13	R6	Input	TDI
14	N/A	Power	1.8 V
15	N/A	Input	VPP

2.1.1 JTAG Interface

The pin assignments for the JTAG programming interface to the Nano-D connector are highlighted in Table 2-2. The four JTAG signals (Txx) are defined by the IEEE 1149.1 (Standard Test Access Port and Boundary-Scan Architecture) specification. The VPP

input is connected to the programming voltage pin of the non-volatile flash memory that is used to store the FPGA configuration bitstream.

Table 2-2 JTAG Pin Assignments Highlighted

Nano-D Pin	FPGA Pin	Signal Type	Signal Name
1	D23 or P11	Bidirectional or Analog Input	GPIO #1 or XADC_VN
2	D24 or N12	Bidirectional or Analog Input	GPIO #2 or XADC_VP
3	E25	Bidirectional	GPIO #3
4	D25	Bidirectional	GPIO #4
5	F22	Bidirectional	GPIO #5
6	E23	Bidirectional	GPIO #6
7	F24	Input	Trigger
8	N/A	Power	GND
9	N/A	Power	GND
10	N8	Input	TMS
11	L8	Input	TCK
12	R7	Output	TDO
13	R6	Input	TDI
14	N/A	Power	1.8 V
15	N/A	Input	VPP

The VPP input provides data protection to the flash contents. A pull-down resistor on the circuit board holds this pin low unless the VPP input of the JTAG interface is tied to 1.8 V. The flash cannot be programmed while VPP is grounded. The JTAG interface supplies the 1.8 V power source needed to drive the VPP input high. Pin #14 and pin #15 can simply be tied together to enable flash programming. It should be noted that there is also a hardware option to drive VPP high on the circuit board so that the flash can be programmed without the JTAG interface connected. This feature allows the flash to be programmed via software through the FPGA.

2.1.2 GPIO Interface

The pin assignments for the GPIO interface to the Nano-D connector are highlighted in Table 2-3. There is a hardware build option to route the first two GPIO pins to the XADC input of the FPGA as shown in Figure 2-4. The default hardware configuration is to route those pins as GPIO #1 and #2 through the translator.

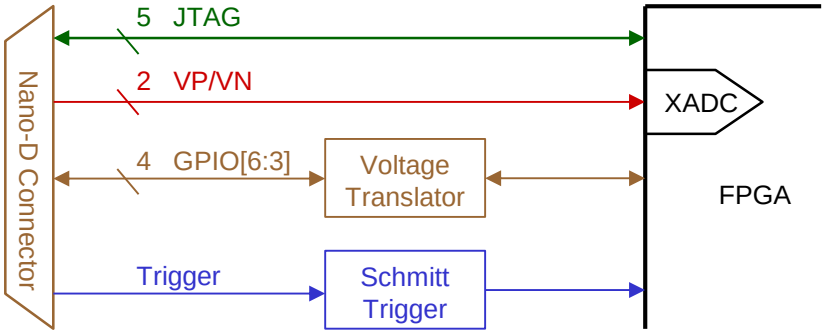


Figure 2-4 Optional Analog XADC Connections

Table 2-3 GPIO Pin Assignments Highlighted

Nano-D Pin	FPGA Pin	Signal Type	Signal Name
1	D23 or P11	Bidirectional or Analog Input	GPIO #1 or XADC_VP
2	D24 or N12	Bidirectional or Analog Input	GPIO #2 or XADC_VN
3	E25	Bidirectional	GPIO #3
4	D25	Bidirectional	GPIO #4
5	F22	Bidirectional	GPIO #5
6	E23	Bidirectional	GPIO #6
7	F24	Input	Trigger
8	N/A	Power	GND
9	N/A	Power	GND
10	N8	Input	TMS
11	L8	Input	TCK
12	R7	Output	TDO
13	R6	Input	TDI
14	N/A	Power	1.8 V
15	N/A	Input	VPP

The GPIO pins are connected to the FPGA through bidirectional voltage translators (Fairchild PN FXL2TD245). The electrical characteristics presented at the Nano-D connector are listed in Table 2-4.

Table 2-4 GPIO Electrical Characteristics

Symbol	Description	MIN	MAX
V_{IH}	High Level Input Voltage	2.0 V	N/A
V_{IL}	Low Level Input Voltage	N/A	0.8 V
I_{OL}, I_{OH}	Output Current	N/A	±24 mA
V_{OH}	I_{OH} = MAX	2.2 V	N/A
V_{OL}	I_{OL} = MAX	N/A	0.55 V
t_{IPLH}, t_{IPHL}	Input Propagation Delay	0.5 ns	5.4 ns
t_{OPLH}, t_{OPHL}	Output Propagation Delay	0.3 ns	4.0 ns
C_{IO}	Input/Output Capacitance	5.0 pF (typical)	

The voltage translator presents a high impedance input to incoming signals. There is a hardware option to add a termination resistor between the signal and ground if different input impedance is required as shown in Figure 2-5. The resistors are added in pairs as shown in the figure.

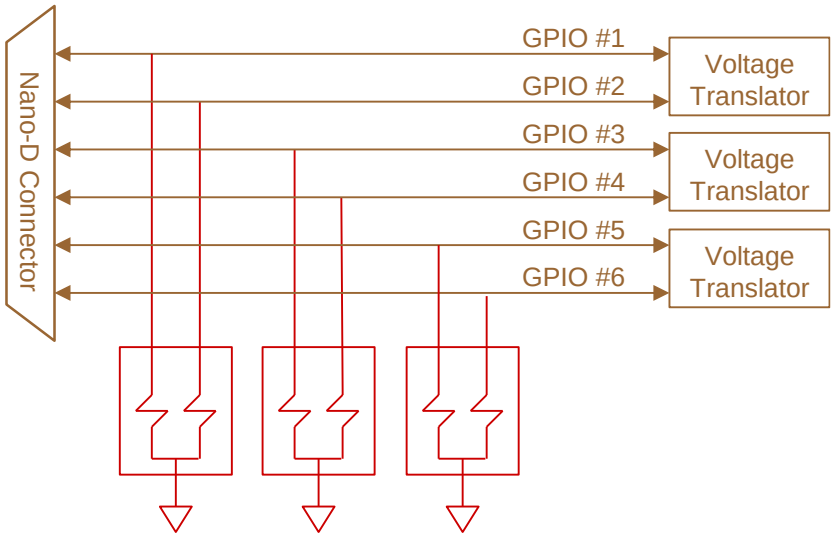


Figure 2-5 Optional GPIO Termination Resistors

There is a hardware option to bypass the voltage translator on every odd/even GPIO pair so that they connect directly to the FPGA as a differential LVDS input. An external termination resistor is also added at the FPGA input as shown in Figure 2-6. It is not possible to use these pairs as an LVDS output since the FPGA I/O bank is powered by 1.8 V. There is no requirement to convert all of the signal pairs to LVDS. The LVDS pairs can be mixed with LVTTL GPIO signals on other connector pins.

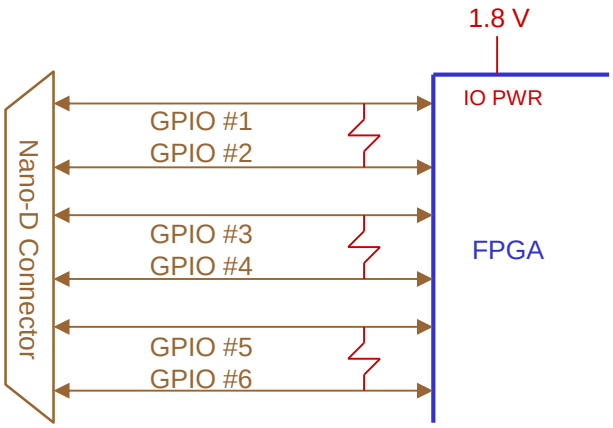


Figure 2-6 Optional Differential Inputs

2.1.3 GPIO Trigger Interface

The trigger pin assignments to the Nano-D connector are highlighted in Table 2-5.

Table 2-5 Trigger Pin Assignments Highlighted

Nano-D Pin	FPGA Pin	Signal Type	Signal Name
1	D23 or P11	Bidirectional or Analog Input	GPIO #1 or XADC_VN
2	D24 or N12	Bidirectional or Analog Input	GPIO #2 or XADC_VP
3	E25	Bidirectional	GPIO #3
4	D25	Bidirectional	GPIO #4
5	F22	Bidirectional	GPIO #5
6	E23	Bidirectional	GPIO #6
7	F24	Input	Trigger
8	N/A	Power	GND
9	N/A	Power	GND
10	N8	Input	TMS
11	L8	Input	TCK
12	R7	Output	TDO
13	R6	Input	TDI
14	N/A	Power	1.8 V
15	N/A	Input	VPP

The trigger pin is connected to the FPGA through a 5 V tolerant Schmitt Trigger (Texas Instrument PN 74LVC1G17) with the input terminated to 50 ohms. The electrical characteristics presented at the Nano-D connector are listed in Table 2-6.

Table 2-6 GPIO Trigger Electrical Characteristics

Symbol	Description	MIN	MAX
V_{T+}	Positive Going Input Threshold	0.76 V	1.13 V
V_{T-}	Negative Going Input Threshold	0.35 V	0.59 V
$V_{T+} - V_{T-}$	Hysteresis	0.36 V	0.64 V
t_{PD}	Propagation Delay	2.8 ns	9.9 ns
t_{OPLH}, t_{OPHL}	Output Propagation Delay	0.3 ns	4.0 ns
C_I	Input Capacitance	4.5 pF (typical)	

3.0 SMA Connector

The circuit board mounted SMA coax connector, shown in Figure 3-1, provides a controlled impedance input trigger to the FPGA. The specific style of connector found on a particular product will depend on whether it is convection or conduction cooled. The SMA will be labeled TRIG on products that include a bezel or face plate. Some products offer the coax trigger input as a build option due to space constraints. These products allow a single connector to function as either a trigger or an external clock/reference input.

Convection Cooled Conduction Cooled

Figure 3-1 SMA Connector

SMA cables are readily available from a wide range of suppliers. The RG316 cable shown in Figure 3-2 is just one example.

Figure 3-2 SMA Cable

3.1 SMA Pinout

The center conductor of the SMA connector is wired to the FPGA as shown in Figure 3-3. The case of the connector is wired to ground.

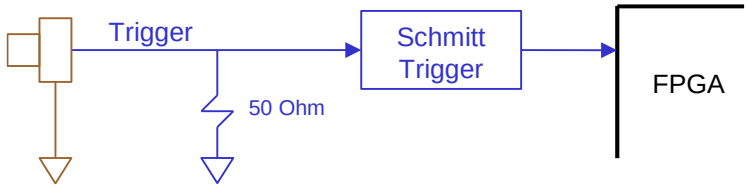


Figure 3-3 SMA Connector Wiring

3.1.1 Coax Trigger Interface

The trigger input is connected to FPGA pin G24 through a 5 V tolerant Schmitt Trigger (Texas Instrument PN 74LVC1G17) with the input terminated to 50 ohms. The FPGA pin assignment is also supplied in a Xilinx Design Constraints (XDC) file that is distributed with the product FPGA development kit.

The electrical characteristics presented at the SMA connector are listed in Table 3-1.

Table 3-1 Coax Trigger Electrical Characteristics

Symbol	Description	MIN	MAX
V_{T+}	Positive Going Input Threshold	0.76 V	1.13 V
V_{T-}	Negative Going Input Threshold	0.35 V	0.59 V
$V_{T+} - V_{T-}$	Hysteresis	0.36 V	0.64 V
t_{PD}	Propagation Delay	2.8 ns	9.9 ns
t_{OPLH}, t_{OPHL}	Output Propagation Delay	0.3 ns	4.0 ns
C_I	Input Capacitance	4.5 pF (typical)	

4.0 LED Indicators

There are two light emitting diodes (LEDs) located on either side of the Nano-D connector as shown in Figure 4-1. These diodes can be toggled on and off through the application logic inside the FPGA. The diodes are not labeled on any bezel or face plate.

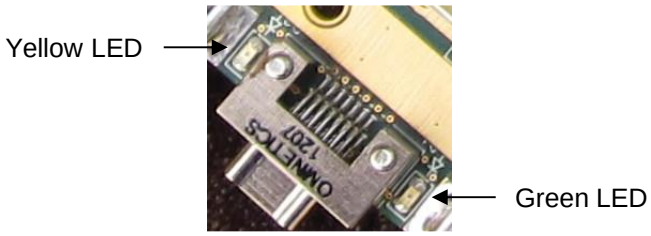


Figure 4-1 LED Positions Adjacent To Nano-D Connector

The yellow LED is connected to FPGA pin A17 and the green is connected to pin B17. The FPGA pin assignments are also supplied in a Xilinx Design Constraints (XDC) file that is distributed with the product FPGA development kit.