15-pin Nano-D Digital Interface

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1.0 Introduction

Products equipped with a customer programmable FPGA include a digital interface connector for discrete utility signals. The same connector is also used to connect an external JTAG programmer to the FPGA. This manual describes the connectivity of a 15-pin Nano-D connector to the FPGA.

The latest product documentation and software is available for download from the Red Rapids website (www.redrapids.com).

1.1 Conventions

This manual uses the following conventions:

☞	Text in this format highlights useful or important information.

!	Text shown in this format is a warning. It describes a situation that could potentially damage your equipment. Please read each warning carefully.

The following are some of the acronyms used in this manual.

- **GPIO** General Purpose I/O
- **JTAG** Joint Test Action Group

1.2 Revision History

Version	Date	Description
R00	3/7/2014	Initial release.

2.0 Nano-D Connector

The circuit board mounted 15-pin Nano-D connector, shown in Figure 2-1, provides a space efficient solution for external digital I/O. Two screws securely attach the connector to the PWB to eliminate strain on the solder connections.

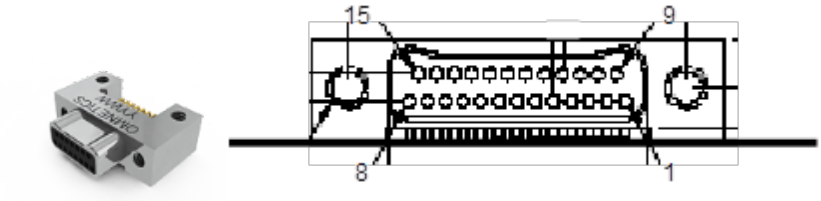
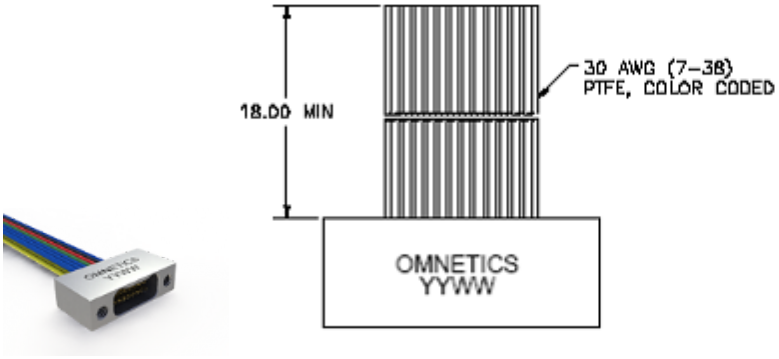


Figure 2-1 15-pin Nano-D Connector

A 15-pin Nano-D pigtail connector mates to the circuit board mounted connector. The connectors are secured using two hex head retention screws. The 30 AWG Teflon coated wires are color coded as shown in Figure 2-2. The pigtail connector assembly is available from Red Rapids or directly from Omnetics (PN A29000-115).



SOCKET	COLOR
1, 11, 21	BLACK
2, 12, 22	BROWN
3, 13, 23	RED
4, 14, 24	ORANGE
5, 15, 25	YELLOW
6, 16	GREEN
7, 17	BLUE
8, 18	VIOLET
9, 19	GRAY
10, 20	WHITE

Figure 2-2 15-pin Nano-D Pigtail

3.0 Connector Pinout

The Nano-D connector supports two different FPGA functions as shown in Figure 2-2. Five pins are allocated to the JTAG programming interface and seven pins are allocated to the GPIO and trigger interfaces. The remaining pins are assigned to power and ground.

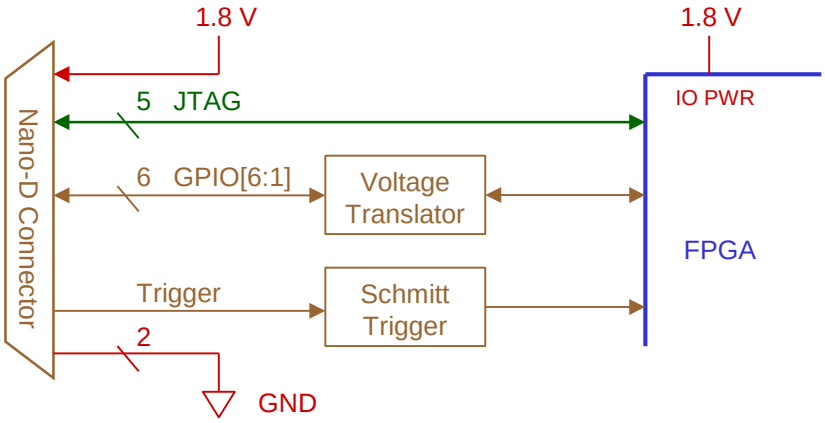


Figure 3-1 Nano-D Connector Pinout

3.1 JTAG Interface

The pin assignments for the JTAG programming interface to the Nano-D connector are shown in Table 3-1. The four JTAG signals (Txx) are defined by the IEEE 1149.1 (Standard Test Access Port and Boundary-Scan Architecture) specification. The VPP input is connected to the programming voltage pin of the non-volatile flash memory that is used to store the FPGA configuration bitstream.

Table 3-1 JTAG Pin Assignments

Pin	Signal Type	Signal Name
8	Power	GND
9	Power	GND
10	Input	TMS
11	Input	TCK
12	Output	TDO
13	Input	TDI
14	Power	1.8 V
15	Input	VPP

The VPP input provides data protection to the flash contents. A pull-down resistor on the circuit board holds this pin low unless the VPP input of the JTAG interface is tied to 1.8 V. The flash cannot be programmed while VPP is grounded. The JTAG interface supplies the 1.8 V power source needed to drive the VPP input high. Pin #14 and pin #15 can simply be tied together to enable flash programming. It should be noted that there is also a hardware option to tie VPP high on the circuit board so that the flash can be programmed without the JTAG interface connected. In this case, the VPP input can either be connected to 1.8 V or left floating for JTAG programming.

3.2 GPIO Interface

The pin assignments for the GPIO interface to the Nano-D connector are shown in Table 3-2. There are six bidirectional digital signals and one trigger input.

Table 3-2 GPIO Pin Assignments

Pin	Signal Type	Signal Name
1	Bidirectional or Analog Input	GPIO #1 or XADC_VN
2	Bidirectional or Analog Input	GPIO #2 or XADC_VP
3	Bidirectional	GPIO #3
4	Bidirectional	GPIO #4
5	Bidirectional	GPIO #5
6	Bidirectional	GPIO #6
8	Power	GND
9	Power	GND

There is a hardware option to route the first two GPIO pins to the XADC input of the FPGA, making those pins unavailable as digital GPIO. Figure 3-2 illustrates the differentical analog connection to the FPGA XADC.

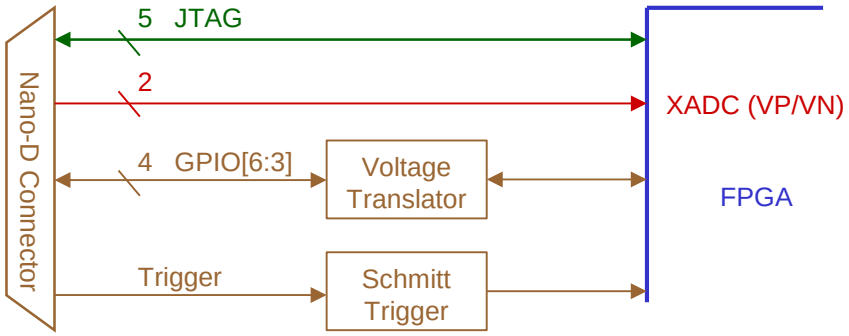


Figure 3-2 Optional Analog XADC Connections

The GPIO pins are connected to the FPGA through bidirectional voltage translators. The electrical characteristics presented at the Nano-D connector are listed in Table 3-3.

Table 3-3 GPIO Electrical Characteristics

Symbol	Description	MIN	MAX
V_{IH}	High Level Input Voltage	2.0 V	N/A
V_{IL}	Low Level Input Voltage	N/A	0.8 V
I_{OL}, I_{OH}	Output Current	N/A	±24 mA
V_{OH}	I_{OH} = -24 mA	2.2 V	N/A
V_{OH}	I_{OH} = -18 mA	2.4 V	N/A
V_{OL}	I_{OL} = 24 mA	N/A	0.55 V
V_{OL}	I_{OL} = 18 mA	N/A	0.4 V
t_{IPLH}, t_{IPHL}	Input Propagation Delay	0.5 ns	5.4 ns
t_{OPLH}, t_{OPHL}	Output Propagation Delay	0.3 ns	4.0 ns
C_{IO}	Input/Output Capacitance	5.0 pF (typical)	

The voltage translator presents a high impedance input to incoming signals. There is a hardware option to add a termination resistor between the signal and ground if different input impedance is required as shown in Figure 3-3. The resistors are added in pairs as shown in the figure.

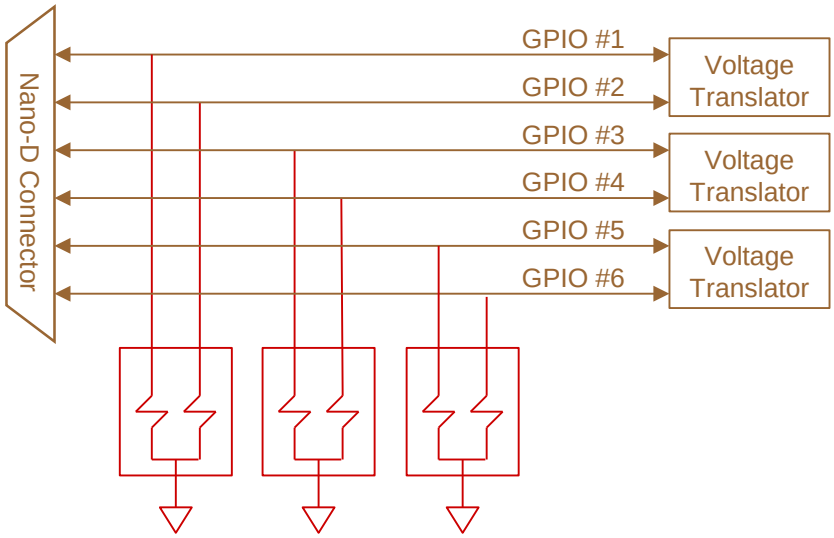


Figure 3-3 Optional GPIO Termination Resistors

There is a hardware option to bypass the voltage translator on every odd/even GPIO pair so that they connect directly to the FPGA as a differential LVDS input. An external termination resistor is also added at the FPGA input as shown in Figure 3-4. It is not possible to use these pairs as an LVDS output since the FPGA I/O bank is powered by 1.8 V. There is no requirement to convert all of the signal pairs to LVDS. The LVDS pairs can be mixed with LVTTL GPIO signals on other connector pins.

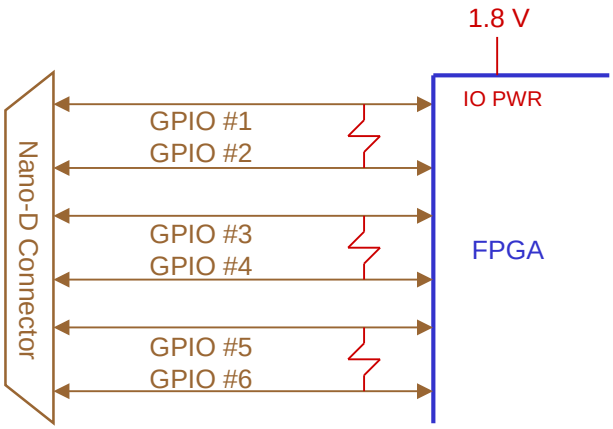


Figure 3-4 Optional Differential Inputs

3.3 Trigger Interface

The trigger pin assignment to the Nano-D connector is shown in Table 3-1.

Table 3-4 Trigger Pin Assignment

Pin	Signal Type	Signal Name
7	Input	Trigger
8	Power	GND
9	Power	GND

The trigger pin is connected to the FPGA through a 5 V tolerant Schmitt Trigger with the input terminated to 50 ohms. The electrical characteristics presented at the Nano-D connector are listed in Table 3-5.

Table 3-5 Trigger Electrical Characteristics

Symbol	Description	MIN	MAX
V_{T+}	Positive Going Input Threshold	0.76 V	1.13 V
V_{T-}	Negative Going Input Threshold	0.35 V	0.59 V
$V_{T+} - V_{T-}$	Hysteresis	0.36 V	0.64 V
t_{PD}	Propagation Delay	2.8 ns	9.9 ns
t_{OPLH}, t_{OPHL}	Output Propagation Delay	0.3 ns	4.0 ns
C_I	Input Capacitance	4.5 pF (typical)	

3.1 FPGA Pin Assignments

The FPGA pin assignments are supplied in constraint files that are distributed with the product FPGA development kit.