Front End 000-015
Dual 16-Bit
575/1500 Msps (Data/DAC)
DC 0-3.6V Output
Transmitter
Reference Manual

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1.0 Introduction

1.1 Contents and Structure

This manual describes the Front End 000-008 transmitter hardware. The focus of this manual is the electrical function of the hardware including control structure, signal flow and key components.

The latest product documentation and software is available for download from the Red Rapids web site (www.redrapids.com) by following the Technical Support link.

1.2 Conventions

This manual uses the following conventions:

☞	Text in this format highlights useful or important information.

!	Text shown in this format is a warning. It describes a situation that could potentially damage your equipment. Please read each warning carefully.

The following are acronyms used in this manual.

- **AC** Alternating Current (Greater than 0 Hertz)
- **ADC** Analog to Digital Converter
- **DAC** Digital to Analog Converter
- **dB** Decibels
- **dBFS** Decibels Relative to Full Scale
- **dBm** Decibels Relative to One milliwatt
- **DC** Direct Current (0 Hertz)
- **DDR** Double Data Rate
- **FFT** Fast Fourier Transform
- **LVDS** Low Voltage Differential Signaling
- **MHz** Megahertz
- **mV** millivolts
- **Msps** Mega Samples per Second
- **RF** Radio Frequency
- **SFDR** Spur Free Dynamic Range
- **SINAD** Signal-to-Noise and Distortion Ratio
- **SNR** Signal-to-Noise Ratio
- **Vpp** Voltage, peak-to-peak

1.3 Revision History

Version	Date	Description
R00	01/23/2018	Initial release.
R01	02/20/2018	Reference to DAC in section 2.0 should be AD9142A not AD9124A

2.0 Description

The Front End 000-015 transmitter is a high performance dual-channel structure built around the Analog Devices AD9142A 16 bit 575/1500 Msps Dual DAC.

Features[1]:

- Dual Channel
- 16-bit Architecture
- Input Rates up to 575 Msps
- Output Rates up to 1500 Msps
- Complex Fine Resolution NCO Enables Precise Carrier Placement
- Programmable I/Q gain, offset and phase matching
- Built-in Digital Upconversion
- Built-in Inverse SINC Filter
- Optional 5-Pole Output Lowpass Filter
- DC Coupled
- Precision DC offset adjustment

Note [1]: Features listed are mode and build dependent. See specifications and performance sections for more information.

A block diagram of the transmitter is shown in Figure 2-1. The transmitter consists of a dual DAC that outputs two semi-independent analog channels. A transmitter channel consists of a DAC, coupling circuit, signal conditioning filter and SMA connector. Sample data is streamed to the DAC input via the data Interface where it is converted into an analog signal, conditioned and output through a standard SMA RF connector. DAC samples are processed using a high-speed precision clock distributed through a low noise network. The following sections describe each element of the transmitter in detail.

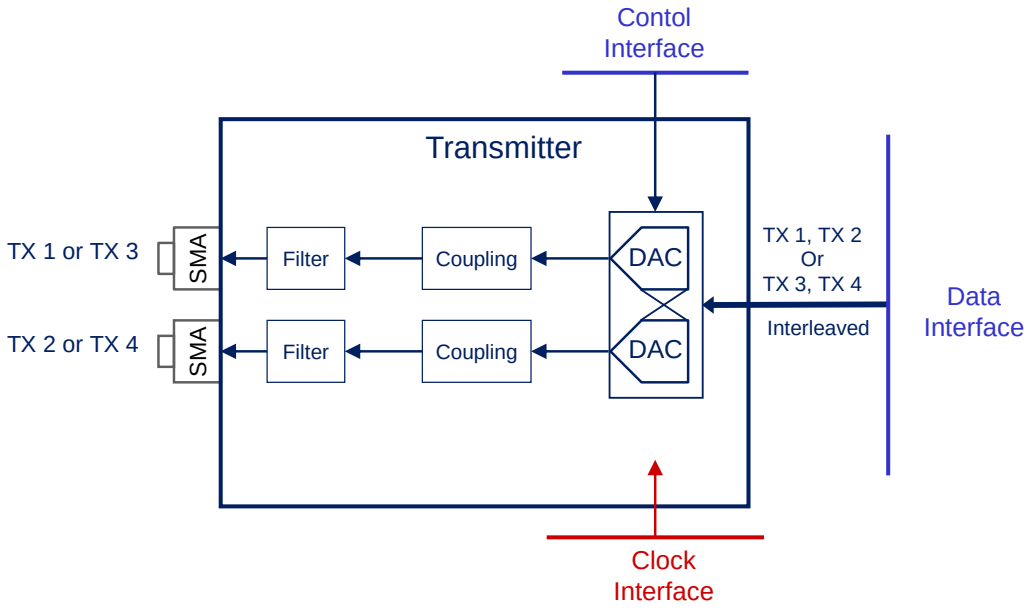

Figure 2-1 Transmitter Block Diagram

The channel numbering for transmit only units is TX 1 and TX 2. Transceiver units are numbered TX 3 and TX 4.

2.1 Coupling

This transmitter variant is DC coupled. DC units use a differential amplifier to couple the signal from the DAC output to the board output as shown in Figure 2-2. The coupling amplifier passes signal frequency content down to DC at the expense of added noise and distortion. The output impedance of the transmitter is extremely low as it is dominated by the coupling amplifier.

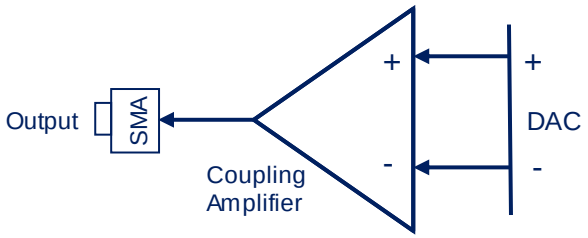

Figure 2-2 Transmitter Coupling

2.2 DC-Offset Adjustment

DC-Coupled units are subject to offsets due to component and system ground level variation. The transmitter provides for analog adjustment of DC-offsets using trim DACs in the push-pull configuration shown in Figure 2-3. Only one trim DAC in the pair should be active at a time. Trim DAC A controls positive offset while DAC B controls negative offset. The transmitter trim DACs are accessed through the Control Interface via a SPI bus as shown in Figure 2-4.Trim DAC register settings can be found in the device data sheet listed in section 5.0.

☞ Only one of the pair of offset trim DACs per input should be active at a time. The unused trim DAC should be set to 0 V.

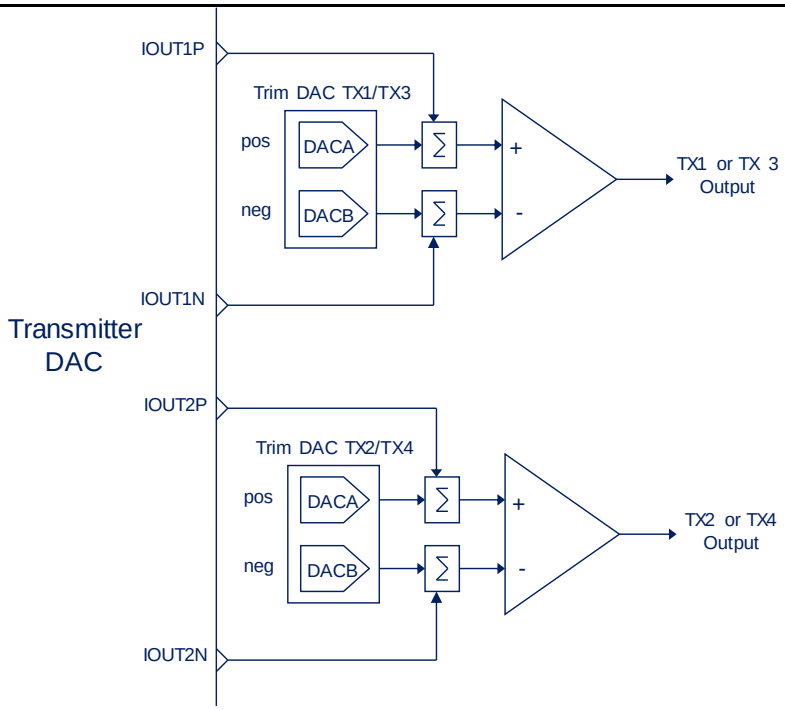

Figure 2-3 DC Offset Adjustment

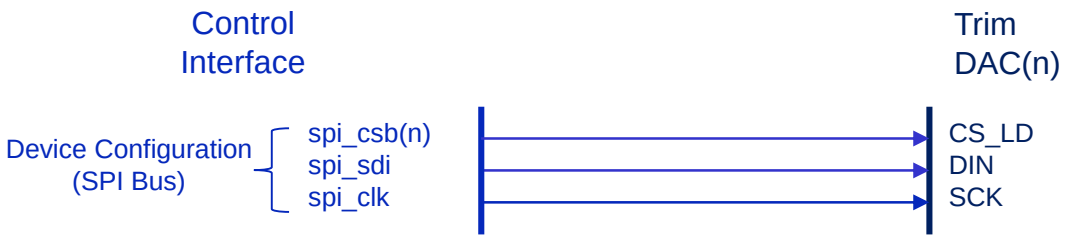

Figure 2-4 Trim DAC Control

2.3 Optional Output Filter

The transmitter features an optional 5-pole lowpass filter at the board output to aid in noise and harmonic distortion reduction as shown in Figure 2-5. Table 2-1 provides a list of filter parameters. The default transmitter build bypasses the output filter to provide maximum frequency response.

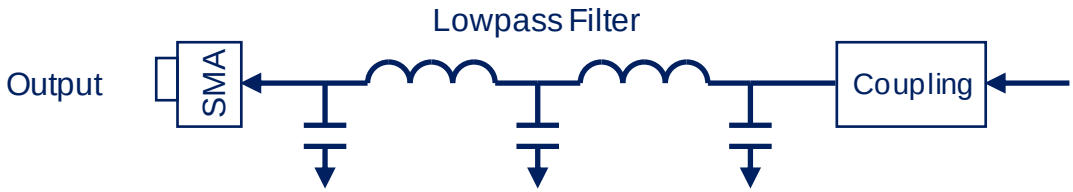

Figure 2-5 Output Filter

Table 2-1 Transmitter Lowpass Filter Build Options

Parameter	Value
Default Build	Bypassed
Filter Type	Chebyshev or Butterworth
Number of Poles	5
3 dB Bandwidth (Cutoff)	10 to 500 MHz
Passband Ripple (Chebyshev)	0.1 dB standard

2.4 Independent Dual Channel vs Complex Mode DAC Operation

The transmitter uses a Dual DAC containing a complex modulator that can be used for frequency translation. The DAC channels must be treated as a complex pair if the complex modulator is enabled by issuing a non-zero frequency tuning command, the same restriction applies to the use of the phase adjustment function. The DAC channels operate as independent channels if the complex modulator is disabled. When operating in complex mode TX1/TX3 is the “I” component and TX2/TX4 is the “Q” component. Use of the interpolator and sinx/x correction modes does not affect the independence of the DAC channels. Please see the transmitter DAC data sheet listed in section 5.0 for configuration information and mode description.

The DAC outputs must be treated as a complex (IQ) pair when using the complex modulator or phase adjustment functions.

2.5 Transmitter DAC Configuration

The transmitter DAC has a number of configuration options available to support different modes of operation. The following sections describe the physical connection of the device in terms of hardwired board connections, clock inputs and control/data interfaces accessible to the user. Operational modes and pin functions are described in the DAC device data sheet listed in section 5.0.

2.5.1 TX DAC Hardware Interface

A diagram of DAC device pin hardware connection is shown in Figure 2-6. The figure shows logical connection of the TX channel interface and individual discrete control pins described in the device data sheet listed in section 5.0.

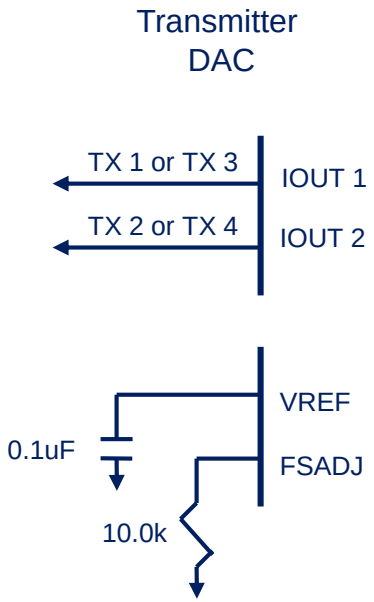

Figure 2-6 TX DAC Hardware Connection

☞	The channel numbering for transmit only units is TX 1 and TX 2. Transceiver units are numbered TX 3 and TX 4.

2.5.2 TX DAC Control Interface

A diagram of DAC control interface is shown in Figure 2-7. The user has access to the DAC command and status registers through a SPI port. In addition, there are several discrete control and status lines available to the user through the control Interface. The transmitter DAC reset is connected directly to the Host System reset pin.

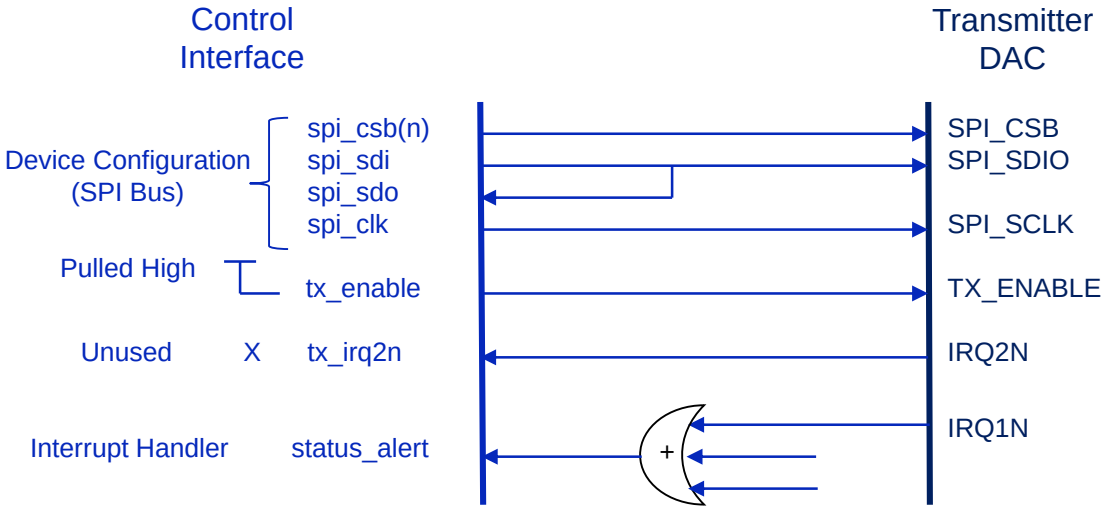

Figure 2-7 TX DAC Control Interface

Figure 2-8 TX DAC Reset

2.5.3 TX DAC Clock Interface

The transmitter DAC clock inputs are sourced by the sample clock distribution network as shown in Figure 2-9.

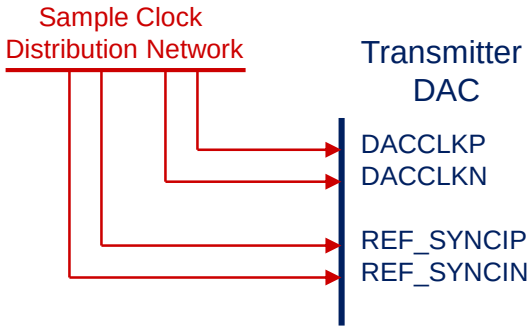

Figure 2-9 TX DAC Clock Interface

2.5.4 TX DAC Data Interface

A diagram of the transmitter DAC data interface is shown in Figure 2-10. The interface consists of an LVDS digital clock input that serves as a double data rate sample clock for the 16-bit LVDS interleaved data channel. An LVDS parity bit is connected to the data interface but is not used. Please see the TX DAC device data sheet in section 5.0 for details.

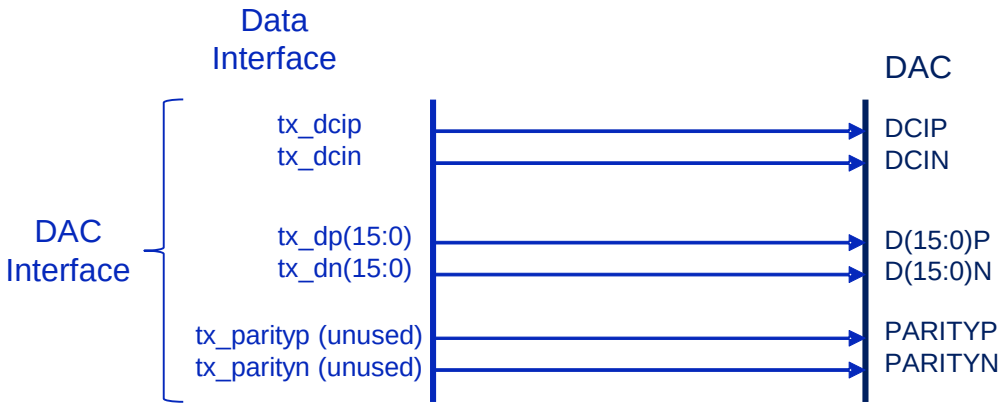

Figure 2-10 TX DAC Data Interface

3.0 Specification

The following section lists the performance specifications of the Front End Transmitter based on direct unit measurement unless otherwise noted. Measurements are listed as typical and represent the mean performance of a representative sample of units under controlled conditions as listed in Table 3-1. More information on test setup can be found in section 4.2. Some variation in performance will occur based on build variation, external system performance and environment. See key component device data sheets in section 5.0 for more insight on performance variation.

Performance may vary depending on the quality of the power supply and EMI environment of the host.

Table 3-1 Test Environment

Item	Description
Host	Personal Computer, Unit on carrier in PCIe x8 Slot
Air Temperature	25 C (Room)
Cooling	Convection (Fan)
Voltage	Nominal “Typical” levels
Register Configuration	Default API from Red Rapids website.
Clock	310 MHz External Clock

3.1 Transmitter Output Levels

Parameter	Min	Typ	Max	Unit
Full Scale output (into 50 ohms)				
Output Voltage range	0		3.6	V
Output Power)			+15	dBm
Offset Adjustment Range(1)	-1.4		+1.4	V

Notes:
(1)Offset adjustment range using DC Trim DACs.

3.2 Transmitter Performance

Measurement conditions: T = 25℃, Supply Voltages (+12, -12, 5, 3.3) nominal

Parameter	Min	Typ	Max	Unit
DAC Input Rate (FData)(1)			575	MHz
DAC Output Rate (FDAC)			1500	MHz
Data Passband(2)				
Real			0.4	FData
Complex			0.8	FData
Analog Passband(3)				
Optimal Performance	DC		FDAC/3	MHz
Limited Performance	FDAC/3		FDAC	MHz
Typical Noise Spectral Density (NSD)				
DC-Coupled		-148		dBm/Hz
SFDR (20.1 MHz +10 dBm Out, FDAC = 1240 MHz)				
<-F0 to < +2F0 (non-harmonic)		85		dBc
2nd Harmonic		49		dBc
3rd Harnonic		52		dBc
Sample Clock Feedthrough				
DC-Coupled		-67		dBm

Notes:
(1)Input data rate determined by sample clock rate.
(2)Usable information bandwidth, DAC SINC response and interpolation image location may reduce effective bandwidth.
(3) DAC performance at frequencies above FDAC/3 are subject to degradation as operating frequencies increase.

3.3 Absolute Maximum Specifications

Stresses above those listed in Table 3-2 may cause damage to the unit. The operation of the unit at these or any other conditions outside of those indicated in the operating sections of this specification is not implied.

Table 3-2 Absolute Maximum Specifications

Parameter	Min	Typ	Max	Unit
Transmitter Output				
Reverse DC Voltage				
DC Coupled	-5V		+5	V

! Exposure to absolute maximum conditions for extended periods may degrade unit reliability.

4.0 Performance

The following sections contain spectrum plots of the transmitter showing typical performance for a sine wave output. Each sine output is characterized using a spectrum analyzer for frequency domain response and an oscilloscope for time domain. Please see section 4.2 for more information on the generation of performance plots.

Table 4-1 Test Environment

Item	Description
Host	Personal Computer, On carrier in PCIe x8 Slot
Air Temperature	25 C (Room)
Cooling	Convection (Fan)
Voltage	Nominal “Typical” levels
Register Configuration	Default API from Red Rapids website.
Clock	310 MHz External Clock

4.1 Performance Plots

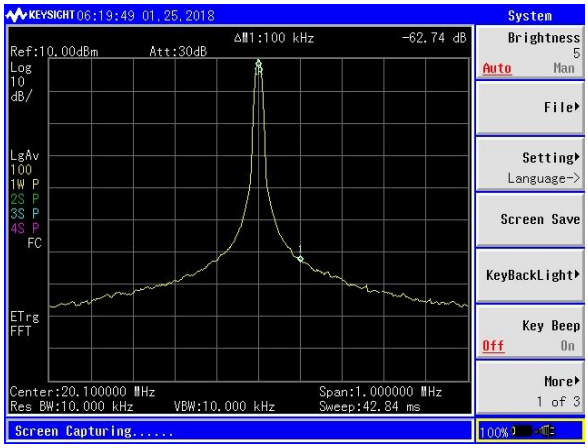

Figure 4-1 20.1 MHz tone, Span 1 MHz

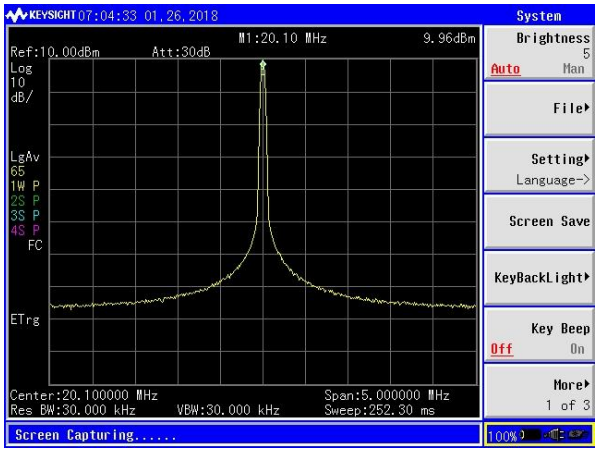

Figure 4-2 20.1 MHz tone, Span 5 MHz

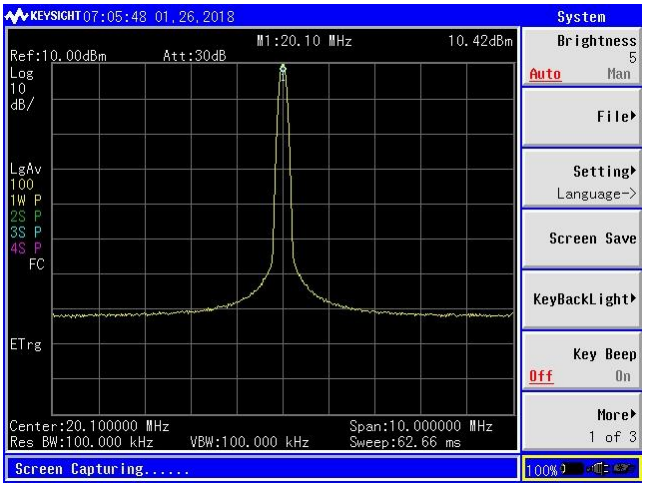

Figure 4-3 20.1 MHz tone, Span 10 MHz

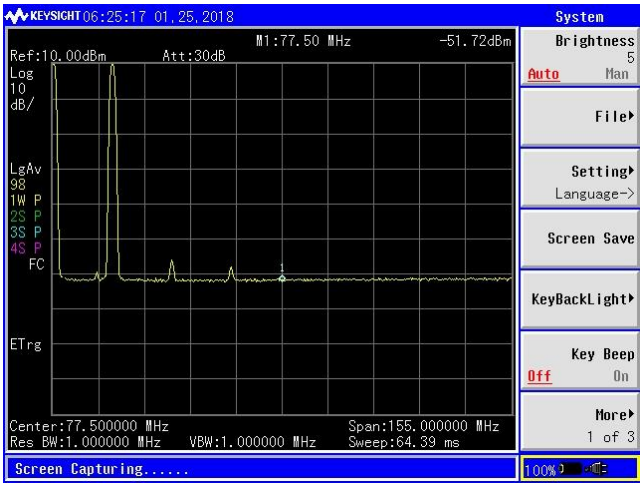

Figure 4-4 20.1 MHz tone, Span 155 MHz

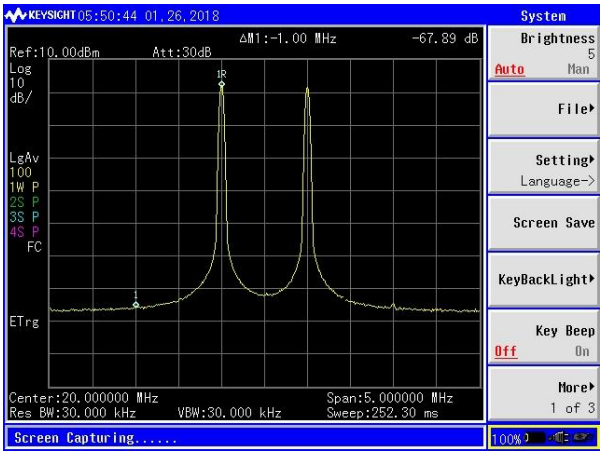

Figure 4-19.5 MHz/20.5 MHz 2-Tone, Span 5 MHz

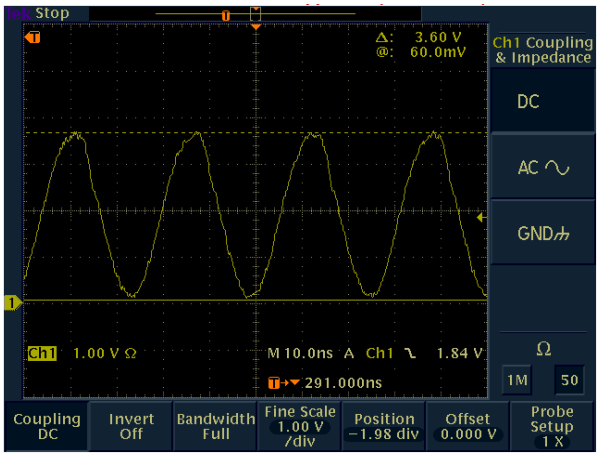

Figure 4-5 38.75 MHz tone, 0-3.6Vpp

4.2 Transmitter Performance Plot Generation

A diagram of the equipment setup used to generate the output plots of section 4.0 is shown in Figure 4-6. Table 4-2 lists the test equipment used to generate the characterization plots. Frequency domain performance plots are screen shots captured on a spectrum analyzer. Time domain performance plots are screen shots captured from an oscilloscope.

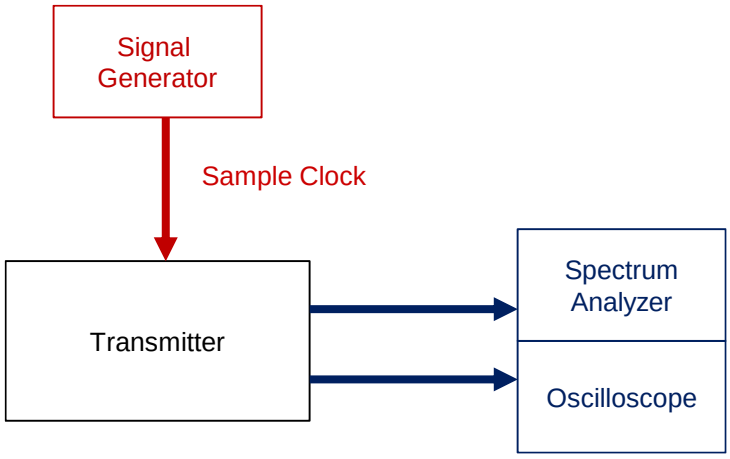

Figure 4-6 Characterization Setup

Table 4-2 Characterization Test Equipment

Function	Part Number	Manufacturer
Sample Clock Source	HP8648B	Agilent
Spectrum Analyzer	N9340B	Agilent
Oscilloscope	TDS3052B	Tektronix

5.0 Key Components

Key hardware components for the Transmitter are listed in Table 5-1. Device datasheets can be downloaded from vendor websites for more information.

Table 5-1 Key Hardware Components

Component	Part Number	Vendor	Comments
Transmitter DAC	AD9142A	Analog Devices	Dual 16-bit 1600 Msps TxDAC+ Digital-to-Analog Converter
Trim DAC	LTC1661	Linear Tech	Micropower Dual 10-bit DAC

6.0 Technical Support

Please feel free to contact us if you have a technical question about or problem with our product. We understand that our customers have tight deadlines and time is of the essence in development and production cycles. We will make every effort to resolve problems as quickly as possible.

Web: www.redrapids.com

Email: support@redrapids.com

Phone: 972-671-9570

Fax: 972-671-9572

Please include the following information with your correspondence:

- Contact Information
- Product Model
- Host Card or System (PC, PCI Carrier, Single Board Computer)
- Operating System
- Problem Description