Front-End 000-011
Octal 16-Bit 125 Msps Receiver
Reference Manual

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Table of Contents

List of Figures

List of Tables

1.0 Introduction

1.1 Contents and Structure

This manual describes the Front-End 000-011 receiver hardware. The focus of this manual is the electrical function of the hardware including control structure, signal flow and key components.

The latest product documentation and software is available for download from the Red Rapids web site (www.redrapids.com) by following the Technical Support link.

1.2 Conventions

This manual uses the following conventions:

- Hexadecimal numbers are prefixed by "0x" (e.g. 0x00058C).

☞	Text in this format highlights useful or important information.

!	Text shown in this format is a warning. It describes a situation that could potentially damage your equipment. Please read each warning carefully.

The following are acronyms used in this manual.

- **AC** Alternating Current (Greater than 0 Hertz)
- **ADC** Analog to Digital Converter
- **DAC** Digital to Analog Converter
- **dB** Decibels
- **dBFS** Decibels Relative to Full Scale
- **dBm** Decibels Relative to One milliwatt
- **DC** Direct Current (0 Hertz)
- **FFT** Fast Fourier Transform
- **LVDS** Low Voltage Differential Signaling
- **MHz** Megahertz
- **mV** millivolts
- **MSPS** Mega Samples per Second
- **PGA** Programmable Gain Amplifier
- **RF** Radio Frequency
- **SFDR** Spur Free Dynamic Range
- **SINAD** Signal-to-Noise and Distortion Ratio
- **SNR** Signal-to-Noise Ratio
- **Vpp** Voltage, peak-to-peak

1.3 Revision History

Version	Date	Description
R00	9/20/2016	Initial release.
R01	7/12/18	R01 PWB performance characterization updates, changed input filter option to 5-pole.

2.0 Description

The Front-End 000-011 receiver is a high performance dual-channel structure built around the Analog Devices AD9653 16-bit 125 Msps Quad ADC.

Features[1]:

- Eight Channels
- 16-bit Architecture
- SNR 77 dB
- SFDR 90 dB
- Sample Rate up to 125 Msps
- PGA Front-End (2.0 Vpp or 2.6 Vpp Input)
- 5-Pole Chebyshev or Butterworth lowpass input filter (optional)
- 225 MHz Full Power Bandwidth
- AC or DC Coupled (Build option)
- Precision DC offset adjustment (DC-Coupled option)

Note [1]: Features listed are mode and build dependent. See specifications and performance sections for more information.

A block diagram of the receiver is shown in Figure 2-1. The receiver consists of eight independent analog input channels labeled 1 through 8. A receiver channel consists of a front panel connector, an optional signal conditioning filter and a coupling mechanism (AC or DC) that bridges the analog input to the ADC. Analog inputs are digitized by two quad-channel ADCs that creates discrete data samples and streams them to the data Interface using a high-speed precision clock distributed from a low noise network.

The following paragraphs provide details about each element of the receiver section.

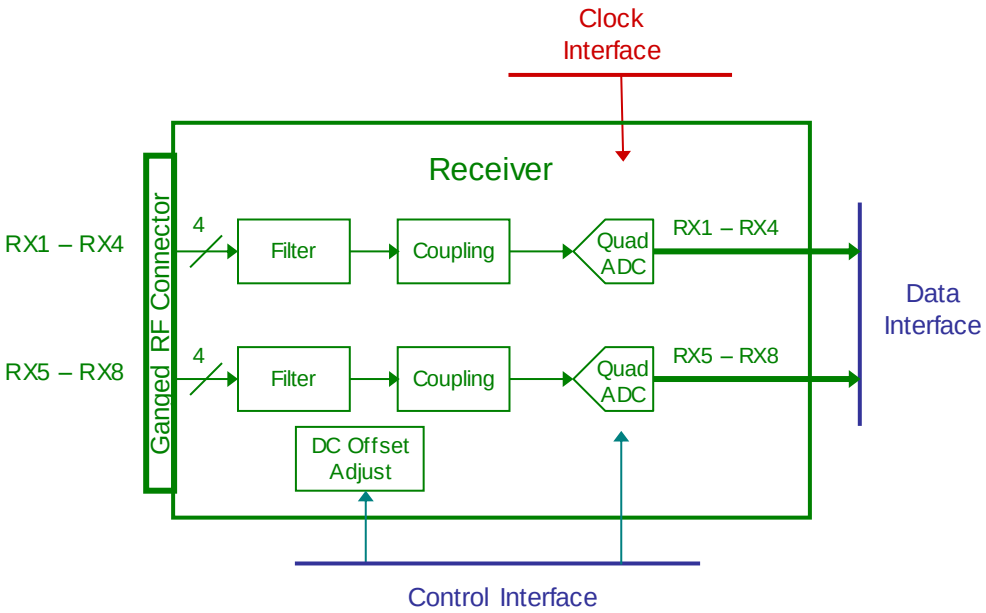


Figure 2-1 Receiver Block Diagram

2.1 Filter Build Option

The Front-End Receiver has two filter build options. The standard build bypasses the filter section to provide maximum frequency response. As an option each receiver is designed to accommodate a 3-pole lumped element single ended Butterworth or Chebyshev lowpass filter. Table 2-1 provides a summary of the filter build option parameters. The filter is located at the receiver input prior to coupling and is useful for limiting broadband noise and harmonic distortion entering the ADC. The default build bypasses the input filter section.

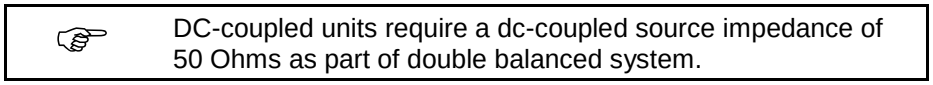
Table 2-1 Lowpass Filter Build Option Parameters

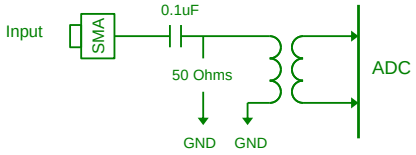
Parameter	Value
Filter Type	Chebyshev or Butterworth
Number of Poles	5
3 dB Bandwidth (Cutoff)	10 to 325 MHz
Passband Ripple (Chebyshev)	0.1 dB standard

2.2 Coupling

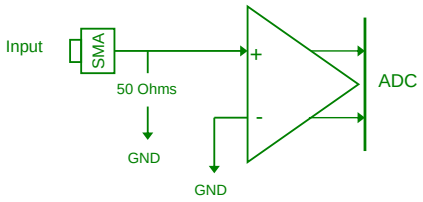
The receiver is available AC or DC coupled as a build option as shown in Figure 2-2. AC coupled units typically offer better high frequency performance and SNR at the expense of low frequency operation. DC-coupled units provide for good mid/low frequency operation down to DC with the expense of added noise and distortion from the coupling amplifier.

AC units block DC signal content with a 0.1 uF series capacitor and are transformer coupled to the ADC. DC-coupled units use a differential amplifier to couple the input signal to the ADC. The differential amplifier also provides signal gain allowing unit operation with a lower input signal amplitude range. DC-coupled units require a dc-coupled system source impedance of 50 Ohms to ensure proper coupling amplifier bias. Other source impedances are supported as a build option.


DC-coupled units require a dc-coupled source impedance of 50 Ohms as part of double balanced system.



AC-Coupled Build Option



DC-Coupled Build Option

Figure 2-2 Coupling Options (equivalent circuits)

2.3 DC Offset Adjustment (DC-Coupled units only)

The DC-coupled receiver option contains a set of DACs to trim larger DC offset errors induced by coupling amplifier and system DC mismatch. The DC offset adjustment structure for one qaud ADC section is shown in Figure 2-3.

> ☞ Only one of the pair of offset trim DACs per input should be active at a time. The unused trim DAC should be set to 0 V.

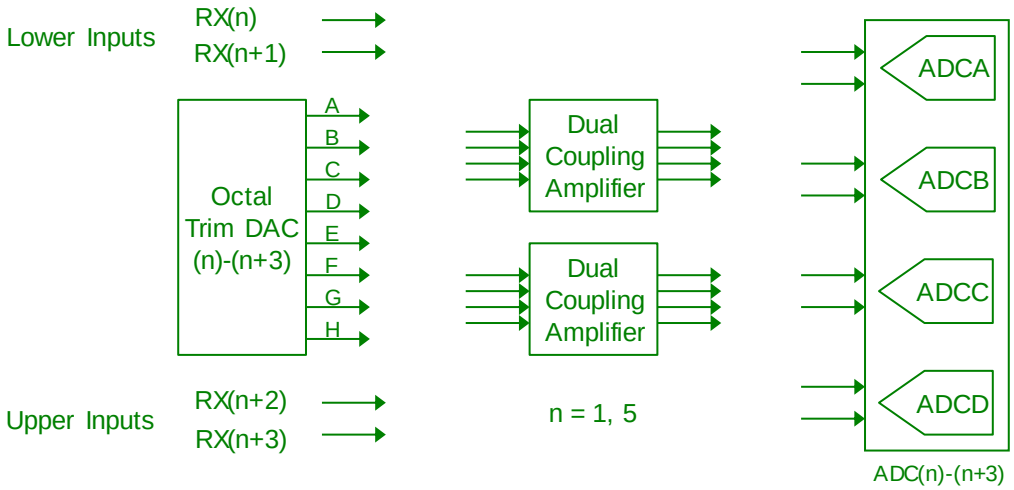


Figure 2-3 DC Offset Adjustment Structure Diagram

Eight offset trim DACs are housed in a single device and operated as four pairs in a "push-pull" configuration as shown in Figure 2-4. DAC "X" offsets the ADC input voltage in a one direction while DAC "Y" offsets the ADC input in the opposite direction. Trim DAC pairing and offset direction information by analog input is listed in Table 2-2. The trim DAC output level is set by user command over the control interface SPI bus. The trim DAC is accessed by asserting the spi_csb(n) for the desired device.

A summary of the trim DAC hardware implementation is provided in Table 2-3. This table describes how the ADC device is physically connected on the printed circuit board. Note that the device defaults to external reference operation and must be configured via the SPI bus to use the internal reference. Please see the trim DAC data sheet listed in 6.0 for more information on device configuration.

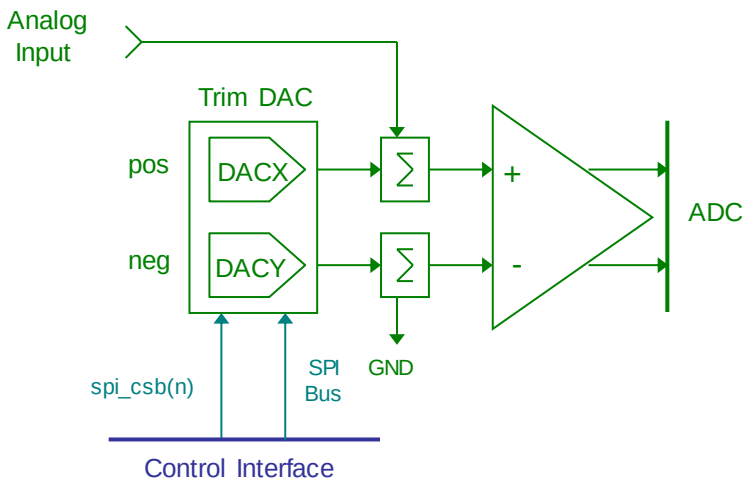


Figure 2-4 Trim DAC Operation in DC-Coupled Build Option

Table 2-2 DC Offset Trim DAC Pairing

Analog Input	Trim DAC Pair	Offset Direction
RX1, RX5	A C	Positive Negative
RX2, RX6	G E	Positive Negative
RX3, RX7	H F	Positive Negative
RX4, RX8	B D	Positive Negative

☞ The Trim DAC defaults to external reference at power up and must be configured via the SPI bus to internal reference mode.

Table 2-3 Trim DAC Physical Connection

Item/DAC Pin	Setting	Connection/Description
Analog Outputs	Output	Tied to coupling amplifier summing nodes
LDAC\	Pulled down	Pulled down (automatic latching)
SYNC\	Control Input	Control interface spi_csb(n)
VREF	Pulled down	Tied to ground through 0.1uF cap. (Internal reference)
CLR\	Pulled up	Pulled up
DIN	Control Input	Control interface SPI_SDIO
SCLK	Control Input	Control interface SPI_SCLK

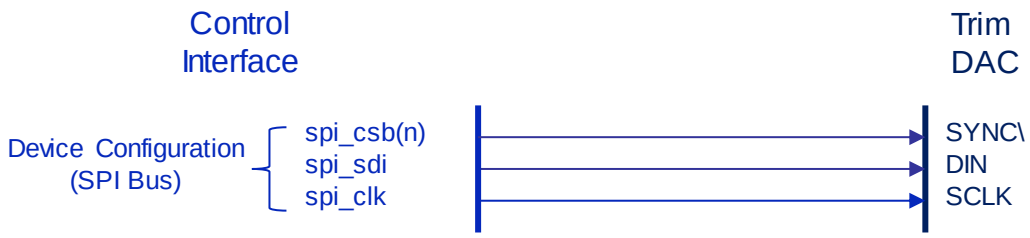


Figure 2-5 Trim DAC Control

2.4 ADC Configuration

The receiver ADC has a number of configuration options available to support different modes of operation. The following sections describe the physical connection of the device in terms of hardwired board connections, clock inputs and control/data interfaces accessible to the user. Operational modes are described in the ADC device data sheet listed in section 6.0. .

2.4.1 ADC Hardware Interface

ADC component physical pin connections are listed in Table 2-4. The table describes logical connection of the RX channel interface and individual discrete control pins described in the device data sheet listed in section 6.0.

Table 2-4 ADC Hardware Configuration

ADC Pin	Setting	Connection/Description
VINA	ADC Input A	RX(n) (n =1 or 5))
VINB	ADC Input B	RX(n+1)
VINC	ADC Input C	RX(n+2)
VIND	ADC Input D	RX(n+3)
DA0/1	ADC Output A	Data interface RX(n)_DA (n =1 or 5).
DB0/1	ADC Output B	Data interface RX(n+1)_DB
DC0/1	ADC Output C	Data interface RX(n+2)_DC.
DD0/1	ADC Output D	Data interface RX(n+3)_DD.
DCO	DCLK Output	Data interface RX(n)-(n+3)_DCLK
FCO	FCLK Output	Data interface RX(n)-(n+3)_FCLK
CLK	Sample Clock	Clock distribution network (ADC Input)
RBIAS	Pull down	10k, 1% pull down resistor.
VCM	Output	Used to bias analog inputs.
SENSE	Pull Down	Pulled down (internal 1.0V reference).
VREF	Decoupled	0.1uF and 1uF parallel pull down.
PDWN	Pulled Down	Pulled down (Power enabled).
SYNC	Control Input	Control interface RX(n)-(n+3)_SYNC
CSB	Control Input	Control interface spi_csb(n)
SDIO	Control Input	Control interface spi_sdio
SCLK	Control Input	Control interface spi_sclk

2.4.1 ADC Control Interface

A diagram of the ADC control interface is shown in Figure 2-6. The user has access to the ADC command and status registers through the control interface SPI port. A list and description of ADC command and status registers can be found in the device data sheet listed in section 6.0.

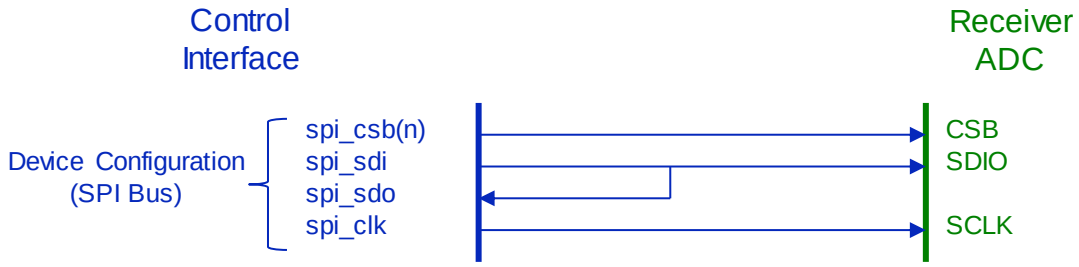


Figure 2-6 ADC Control Interface

2.4.1 ADC Clock Interface

The receiver ADC clock input is sourced by the sample clock distribution network as shown in Figure 2-7.

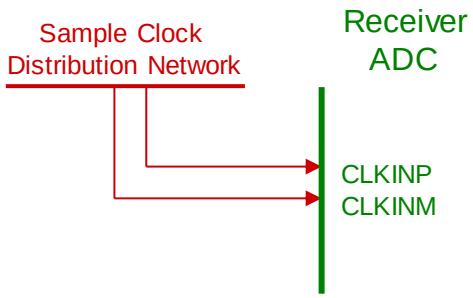


Figure 2-7 ADC Clock Interface

2.4.2 ADC Data Interface

A diagram of the ADC data interface is shown in Figure 2-8. The interface consists of a forwarded LVDS data clock (DCLK), a data frame clock (FCLK) and four sets of 2-bit serial LVDS pairs for data transfer. A description of the data transfer protocol can be found in the RX ADC device data sheet listed in section 6.0.

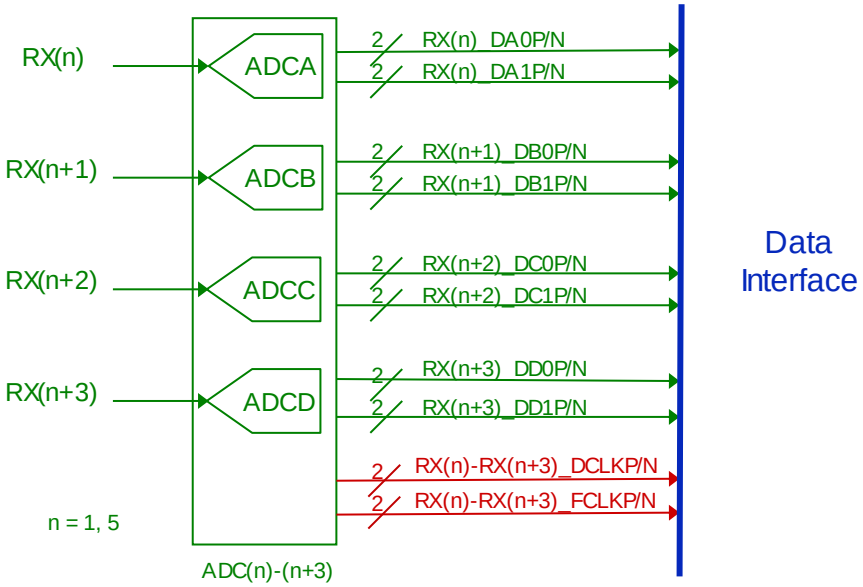


Figure 2-8 ADC Data Interface

3.0 Specifications

The following section lists the performance specifications of the Front-End Receiver based on direct unit measurement unless otherwise noted. Measurements are listed as typical and represent the mean performance of a representative sample of units under laboratory conditions as listed in Table 3-1. More information on test setup can be found in section 5.2. Some variation in performance will occur based on build variation, external system performance and environment. See key component device data sheets in section 6.0 for more insight on performance variation.

Table 3-1 Test Environment

Item	Description
Host	Personal Computer, On carrier in PCIe x8 Slot
Air Temperature	25 C (Room)
Cooling	Convection (Fan)
Voltage	Nominal “Typical” levels
ADC Control	Default API from Red Rapids website.
Clock	125 MHz Internal Clock

3.1.1 Analog Input Levels

Parameter	Min	Typ	Max	Unit
Input Impedance		50		Ohms
ADC Offset Error (2Vpp Input)(1)	-10	-6	+4	mV
Un-calibrated DC Coupling Offset Error(2)	-50	+/-10	+50	mV
ADC Gain Error	-12.3	-5	+2.37	%FS
DC-Coupled Option – DC Offset Control(3)				
Range (at input)	-0.5		+0.5	V
Resolution		500		uV/step
Full Scale Input (0 dBFS, 50 ohms, 20.1 MHz, 1.0 V Vref)				
AC-Coupled Build				
Input Voltage		1.9		Vpp
Input Power		+9.5		dBm
DC-Coupled Build				
Input Voltage		0.95		Vpp
Input Power		+3.5		dBm

Notes: (1) ADC offset dominates when AC coupled, does not include offset compensation
(2) Typical DC offset due to component tolerance, does not include system DC variation.
(3) DC offset adjustment is discussed in section 2.3.

3.1.2 Analog Input Performance

Performance specifications represent the average of measurements taken across a number of channels calculated from a 32k point FFT. The SNR and SINAD measurements represent equivalent full scale performance (dBFS) where the input amplitude is added to the FFT measurement to match the method used in the ADC data sheet. SFDR measurements are relative to the input signal level. Measurements were taken using a -1 dBFS input signal unless otherwise noted.

Performance may vary depending on the quality of the power supply and EMI environment of the host.

3.1.2.1 AC-Coupled Performance Internal Synthesizer

Measurement conditions: T = 25°C, Nominal Supply Voltages

Parameter	Min	Typ	Max	Unit
Passband [1]				
1 dB	1		100	MHz
3 dB	0.1		180	MHz
SNR				
20.17 MHz Input		77.6		dBFS
70.17 MHz Input		73.6		dBFS
124.17 MHz Input		69.3		dBFS
SINAD				
20.17 MHz Input		76.9		dBFS
70.17 MHz Input		73.4		dBFS
124.17 MHz Input		67.7		dBFS
SFDR				
20.17 MHz Input		-85		dBc
70.17 MHz Input		-87		dBc
124.17 MHz Input		-78		dBc
RX Channel to RX Channel Isolation [2]				
1 MHz		86		dB
50 MHz		77		dB
100 MHz		71		dB
150 MHz		68		dB
200 MHz		64		dB

Notes:

[1] Measured across band from ADC output with no filter.

[2] Worst adjacent channel with -1 dBFS input.

3.1.2.2 DC-Coupled Performance Internal Synthesizer

Measurement conditions: T = 25°C, Nominal Supply Voltages

Parameter	Min	Typ	Max	Unit
Passband [1]				
1 dB	DC		70	MHz
3 dB	DC		140	MHz
SNR				
20.17 MHz Input		70.6		dBFS
70.17 MHz Input		68.9		dBFS
124.17 MHz Input		66.1		dBFS
SINAD				
20.17 MHz Input		70.5		dBFS
70.17 MHz Input		68.4		dBFS
124.17 MHz Input		65.0		dBFS
SFDR				
20.17 MHz Input		-88		dBc
70.17 MHz Input		-79		dBc
122.17 MHz Input		-74		dBc
RX Channel to RX Channel Isolation [2]				
1 MHz		99		dB
50 MHz		78		dB
100		72		dB
150 MHz		68		dB
200 MHz		66		dB

Notes:

[1] Measured across band using ADC output with no filter.

[2] Worst adjacent channel with -1 dBFS input.

4.0 Absolute Maximum Specifications

Stresses above those listed in Table 4-1 may cause damage to the unit. The operation of the unit at these or any other conditions outside of those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may degrade unit reliability.

Table 4-1 Absolute Maximum Specifications

Parameter	Min	Typ	Max	Unit
Environmental				
Operating Temperature	0		55	C
Non-Operating Temperature	-30		85	C
Analog Inputs (50 Ohms)				
AC-Coupled				
DC Input Voltage	-10		10	V
AC Voltage Swing			5.0	Vpp
AC Input Power			+18	dBm
DC-Coupled(1)				
DC Offset(1)	-1.0		+1.0	V
AC Voltage Swing(1)			2.0	Vpp
AC Input Power(1)			+10	dBm

(1) DC-offset maximum is the sum of AC swing plus offset. Absolute excursion should not exceed absolute maximum DC offset value.

> **!** Exposure to absolute maximum conditions for extended periods may degrade unit reliability.

5.0 Typical Performance Characteristics (Preliminary)

This section contains frequency response and spectral plots of the Front-End Receiver. These spectral plots provide an indication of receiver performance under controlled conditions. Data is measured with an internal sample clock unless otherwise noted.

5.1 Analog Input Performance using Internal Synthesizer

The following sections contain spectrum plots of the Front-End Receiver showing typical performance for a variety of sine wave inputs. The receiver performance section is divided into AC and DC coupled subsections. Each sine input is characterized using a 32k point FFT. All data was collected using the on-board 125 MHz sample clock.

5.1.1 AC-Coupled

The following receiver plots were taken with the Front-End Receiver configured for AC-coupled operation and no on-board lowpass filter.

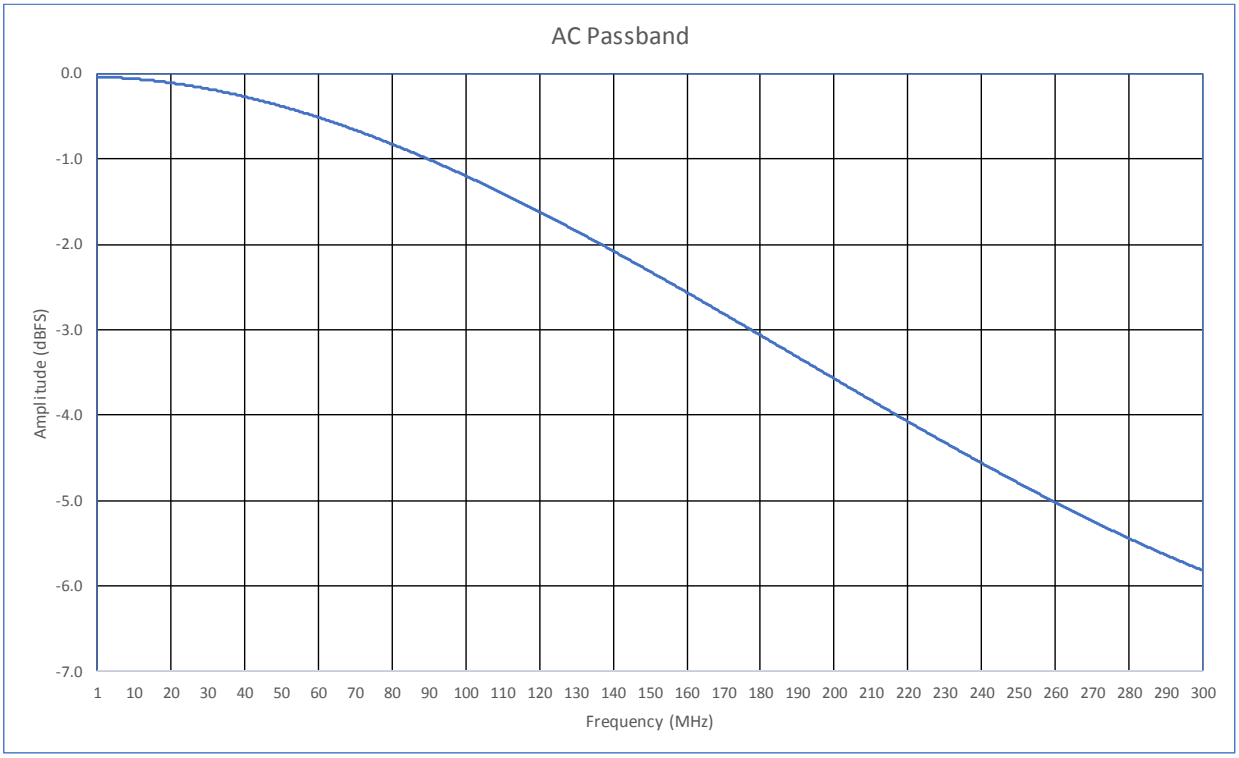


Figure 5-1 Front-End Receiver AC-Coupled Passband Response 1 MHz to 300 MHz

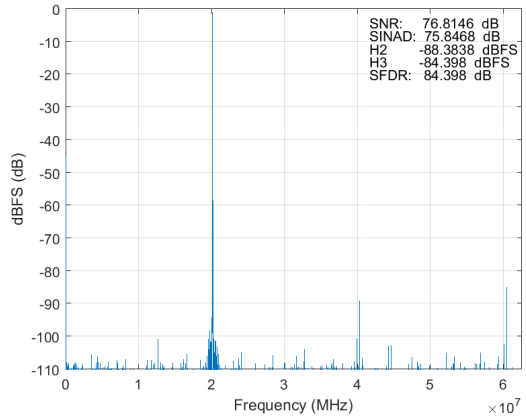


Figure 5-2 20.17 MHz, -1.0dBFS

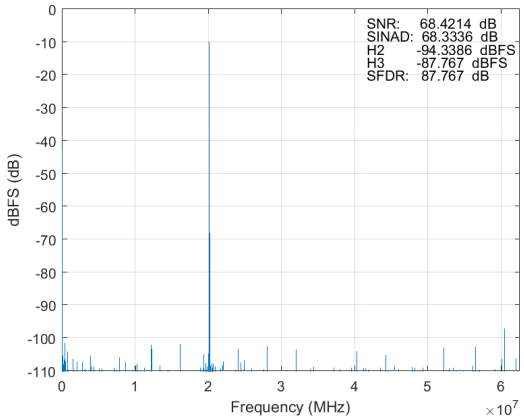


Figure 5-3 20.17 MHz, -10.0dBFS

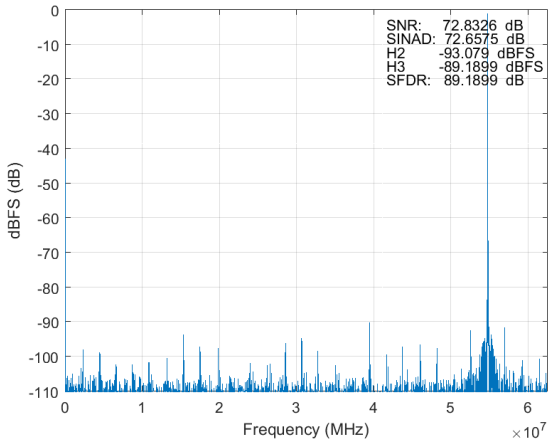


Figure 5-4 70.17 MHz, -1.0 dBFS

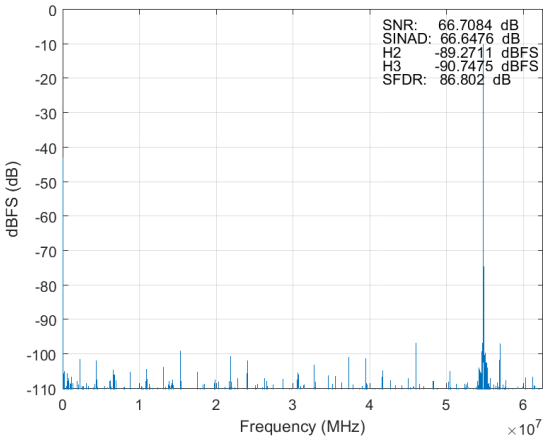


Figure 5-5 70.17 MHz, -10.0 dBFS

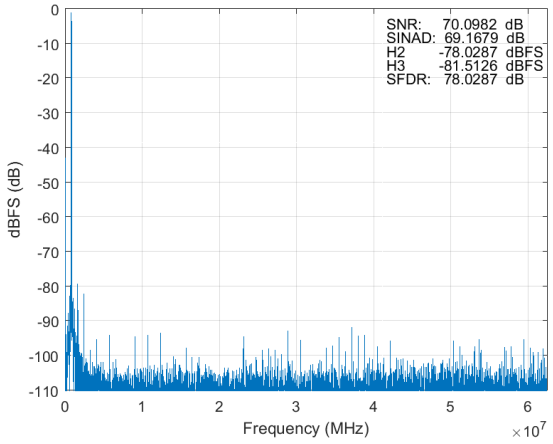


Figure 5-6 124.17 MHz, -1.0 dBFS

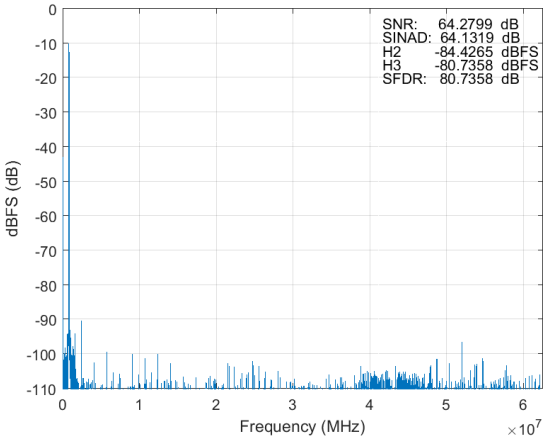


Figure 5-7 124.17 MHz, -10.0 dBFS

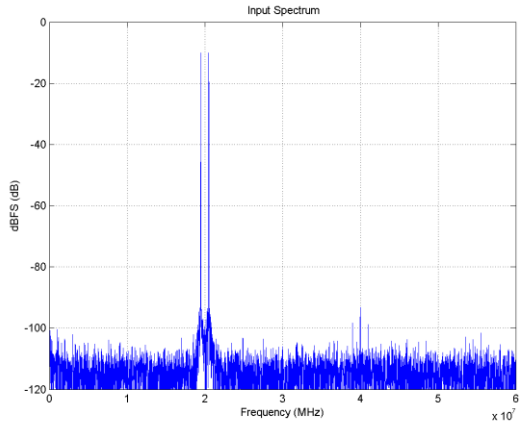


Figure 5-8 2-Tone -10dBFS, 19.5 MHz and 20.5 MHz

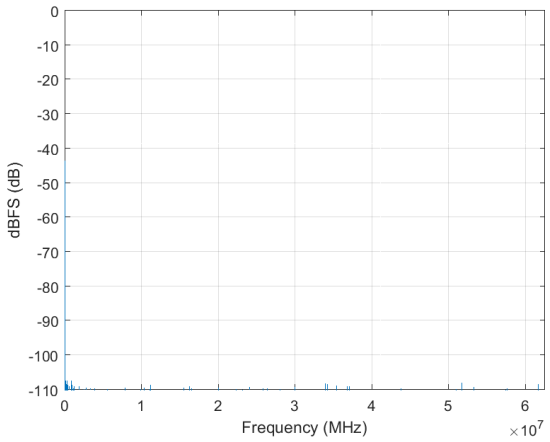


Figure 5-9 Terminated Input

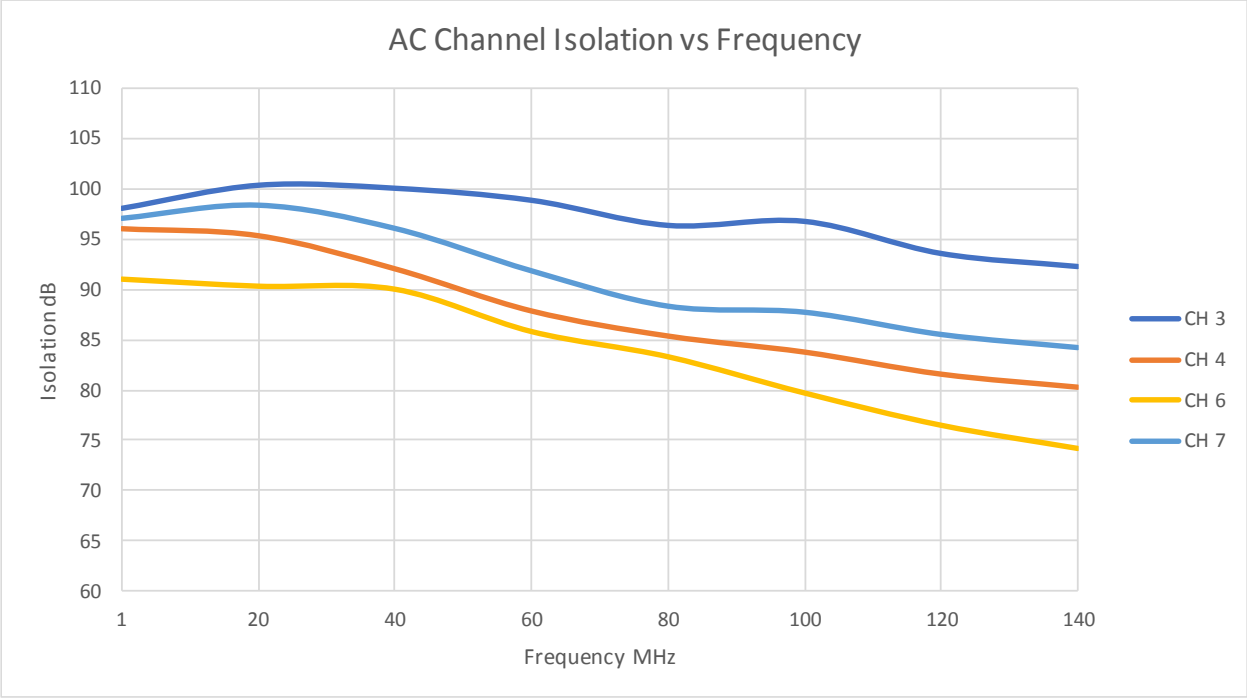


Figure 5-10 AC Channel Isolation vs. Frequency (1)

(1) Interfering signal input in channel 5 at -10 dBFS with isolation measured in terminated channels 3, 4, 6 and 7.

5.1.2 DC-Coupled

The following receiver plots were taken with the Front-End Receiver configured for DC-coupled operation.

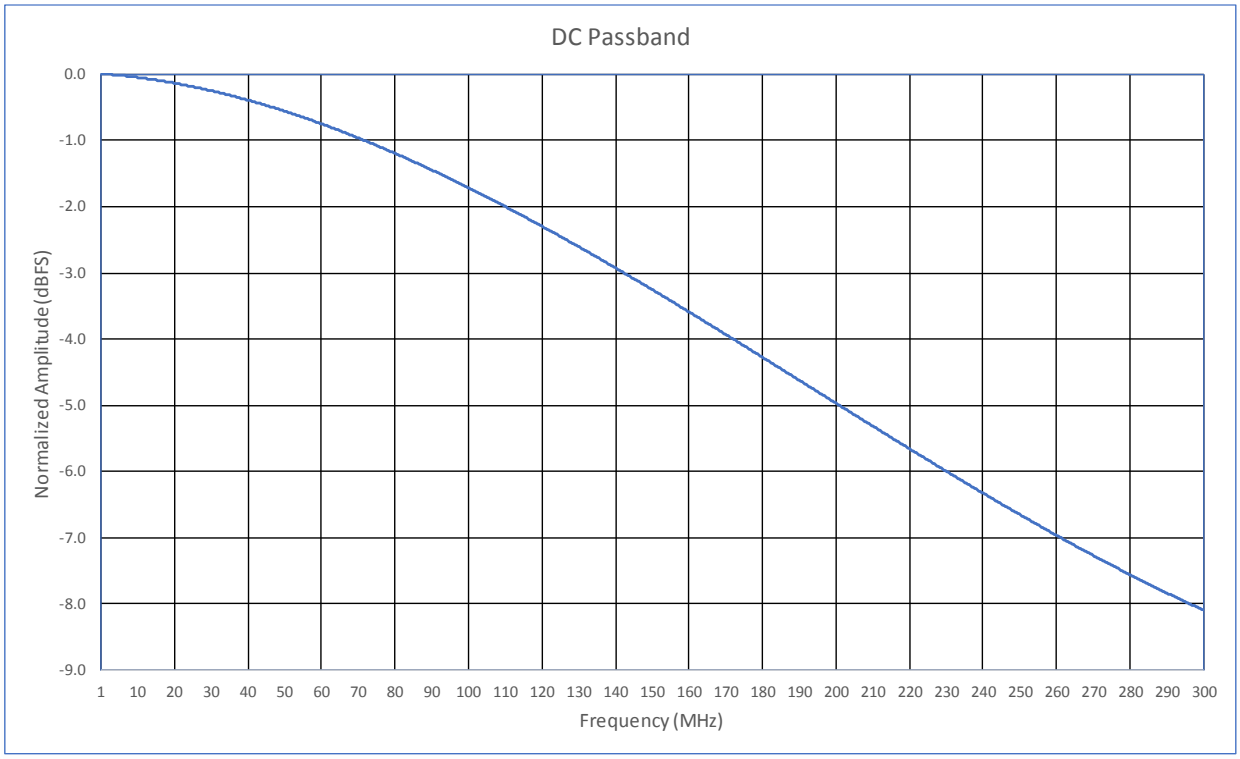


Figure 5-11 DC-Coupled Passband Response DC to 300 MHz

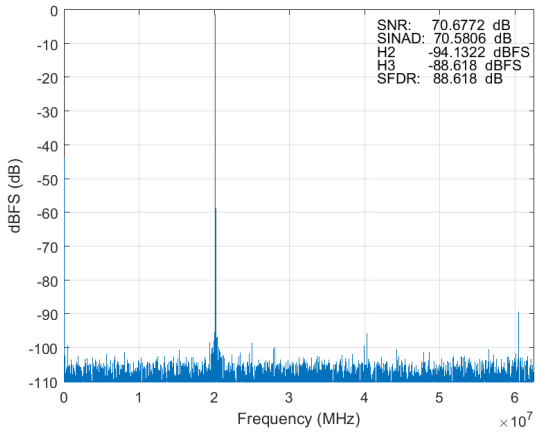


Figure 5-12 20.17MHz, -1.0dBFS

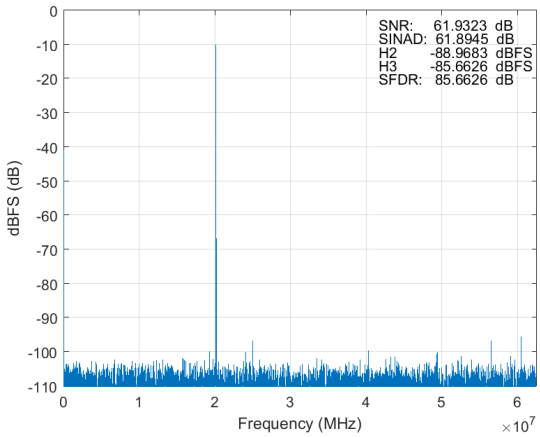


Figure 5-13 20.17MHz, -10.0dBFS,

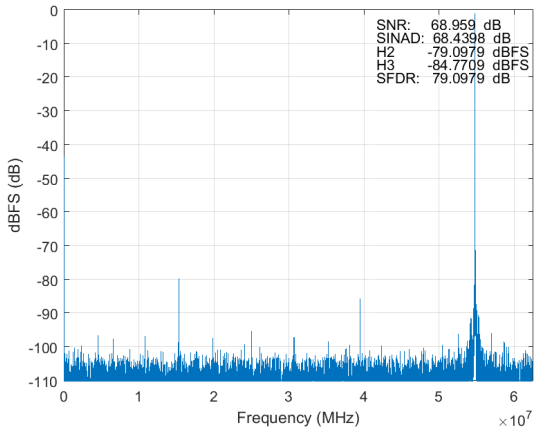


Figure 5-14 70.17MHz, -1.0dBFS

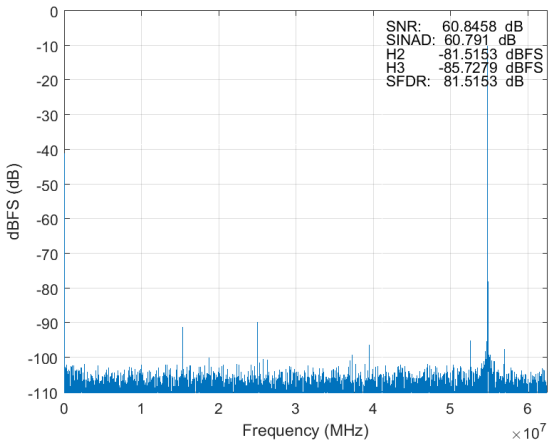


Figure 5-15 70.17MHz, -10.0dBFS

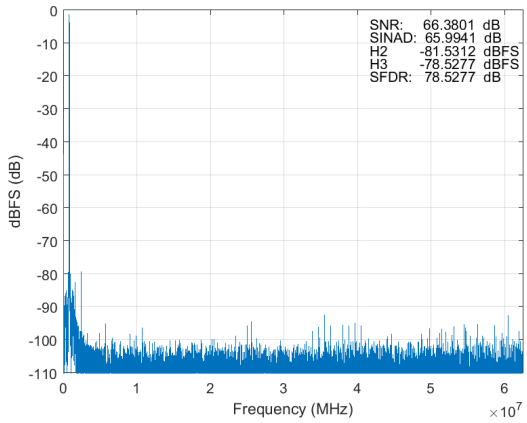


Figure 5-16 124.17 MHz, -1.0 dBFS

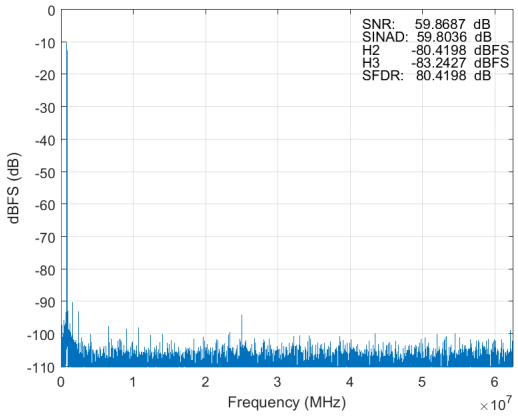


Figure 5-17 125.22MHz, -10.0 dBFS

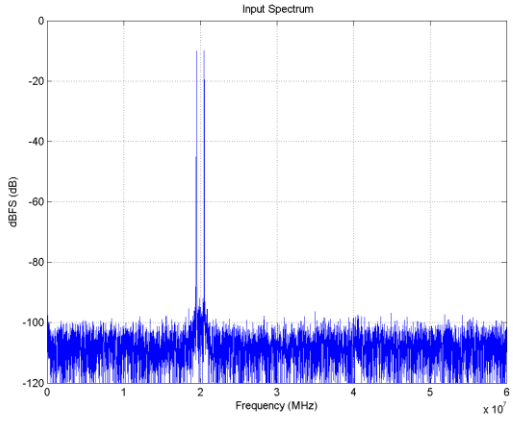


Figure 5-18 2-Tone at -10dBFS, 19.5 MHz and 20.5 MHz

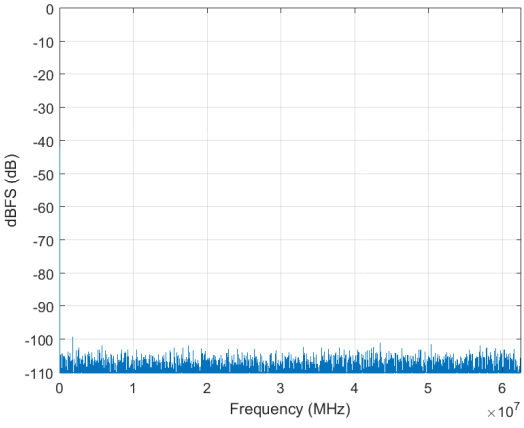


Figure 5-19 Terminated Input

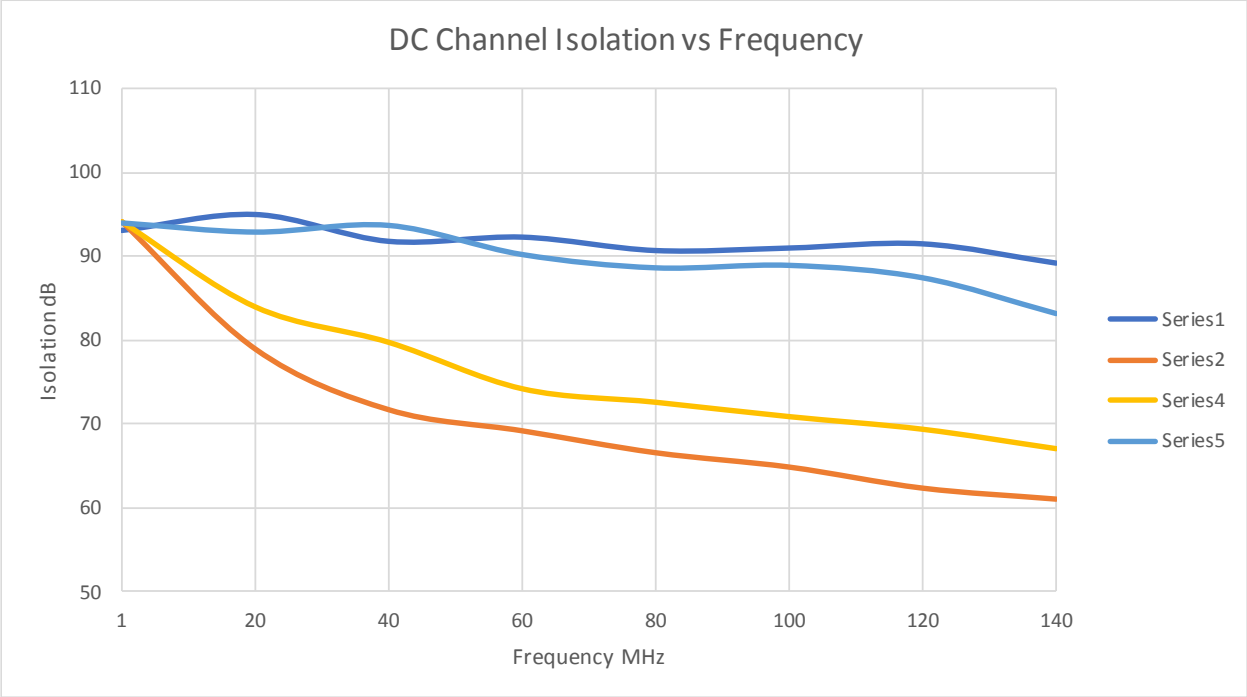


Figure 5-20 DC Channel Isolation vs Frequency (1)

(1) Interfering signal input in channel 5 at -10 dBFS with isolation measured in terminated channels 3, 4, 6 and 7.

5.2 Generating Characterization Plots

The wide dynamic range and input bandwidth characteristics of the receiver levy strict signal conditioning requirements on test equipment used to characterize board performance. Even the highest quality general purpose RF signal generators output harmonics and noise that must be reduced in order to accurately characterize system performance. Generally a narrow bandpass filter is inserted between the signal generator output and the Adapter Module receiver input. The bandpass filter should be reasonably narrow to eliminate generator harmonics and limit the amount of generator phase noise input into the receiver. Red Rapids' characterization plots were created using 5% bandwidth 7-section Chebyshev filters with > 55 dB of stop band rejection. We used filters from TTE such as their KC7t-70m-3.5m-50-720a. Table 5-1 contains a list of test equipment used to generate the characterization plots of section 5.0. The characterization frequency plots were generated by performing a 32k FFT on 32k data samples collected from the receiver.

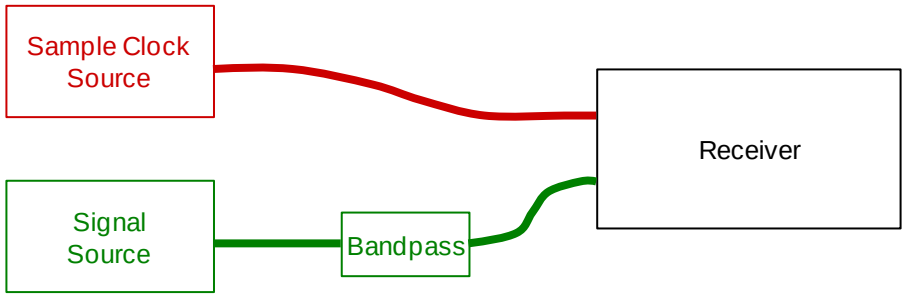


Figure 5-21 Characterization Setup

Use a narrow bandpass filter between the signal generator and receiver card to accurately characterize system.

Table 5-1 Characterization Test Equipment

Function	Part Number	Manufacturer
Sample Clock Source	HP8648B	Agilent
Signal Bandpass Filter (one of several)	KC7t-70m-3.5m-50-720a	TTE
Signal Source	HP8648B	Agilent

6.0 Key Components

Key hardware components for the Receiver are listed in Table 6-1. Device datasheets can be downloaded from vendor websites for more information.

Table 6-1 Key Hardware Components

Component	Part Number	Vendor	Comments
Receiver ADC	AD9653BCPZ-125	Analog Devices	Quad, 16-bit, 125 Msps, serial LVDS, 1.8V, A-D Converter
Trim DAC	AD5628BCPZ-2-RL7	Analog Devices	Octal 12-bit SPI Voltage Output DAC

7.0 Technical Support

Please feel free to contact us if you have a technical question about or problem with our product. We understand that our customers have tight deadlines and time is of the essence in development and production cycles. We will make every effort to resolve problems as quickly as possible.

Web: www.redrapids.com

Email: support@redrapids.com

Phone: 972-671-9570

Fax: 972-671-9572

Please include the following information with your correspondence:

- Contact Information
- Product Model
- Host Card or System (PC, PCI Carrier, Single Board Computer)
- Operating System
- Problem Description