Front End 000-009
Dual 16-Bit 310 Msps Receiver
Reference Manual

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1.0 Introduction

1.1 Contents and Structure

This manual describes the Front End 000-009 receiver hardware. The focus of this manual is the electrical function of the hardware including control structure, signal flow and key components.

The latest product documentation and software is available for download from the Red Rapids web site (www.redrapids.com) by following the Technical Support link.

1.2 Conventions

This manual uses the following conventions:

- Hexadecimal numbers are prefixed by "0x" (e.g. 0x00058C).

☞	Text in this format highlights useful or important information.

!	Text shown in this format is a warning. It describes a situation that could potentially damage your equipment. Please read each warning carefully.

The following are acronyms used in this manual.

- **AC** Alternating Current (Greater than 0 Hertz)
- **ADC** Analog to Digital Converter
- **DAC** Digital to Analog Converter
- **dB** Decibels
- **dBFS** Decibels Relative to Full Scale
- **dBm** Decibels Relative to One milliwatt
- **DC** Direct Current (0 Hertz)
- **FFT** Fast Fourier Transform
- **LVDS** Low Voltage Differential Signaling
- **MHz** Megahertz
- **mV** millivolts
- **MSPS** Mega Samples per Second
- **PGA** Programmable Gain Amplifier
- **RF** Radio Frequency
- **SFDR** Spur Free Dynamic Range
- **SINAD** Signal-to-Noise and Distortion Ratio
- **SNR** Signal-to-Noise Ratio
- **Vpp** Voltage, peak-to-peak

1.3 Revision History

Version	Date	Description
R00	1/21/2016	Initial release.

2.0 Description

The Front End 000-009 receiver is a high performance dual-channel structure built around the Analog Devices AD9652 16 bit 310 Msps dual ADC.

Features[1]:

- Dual Channel
- 16-bit Architecture
- SNR 75 dB
- SFDR 94 dB
- Sample Rate up to 310 Msps
- PGA Front End (2.0 Vpp or 2.5 Vpp Input)
- 3-Pole Chebyshev or Butterworth lowpass input filter (optional)
- 400 MHz Full Power Bandwidth
- AC or DC Coupled (Build option)
- Precision DC offset adjustment (DC-Coupled option)

Note [1]: Features listed are mode and build dependent. See specifications and performance sections for more information.

A block diagram of the receiver is shown in Figure 2-1. The receiver consists of two independent analog input channels labeled 1 and 2. A receiver channel consists of a front panel SMA connector, an optional signal conditioning filter and a coupling mechanism (AC or DC) that bridges the analog input to the ADC. Analog inputs are digitized by a dual ADC that creates discrete data samples and streams them to the data Interface using a high-speed precision clock distributed from a low noise network.

The following paragraphs provide details about each element of the receiver section.

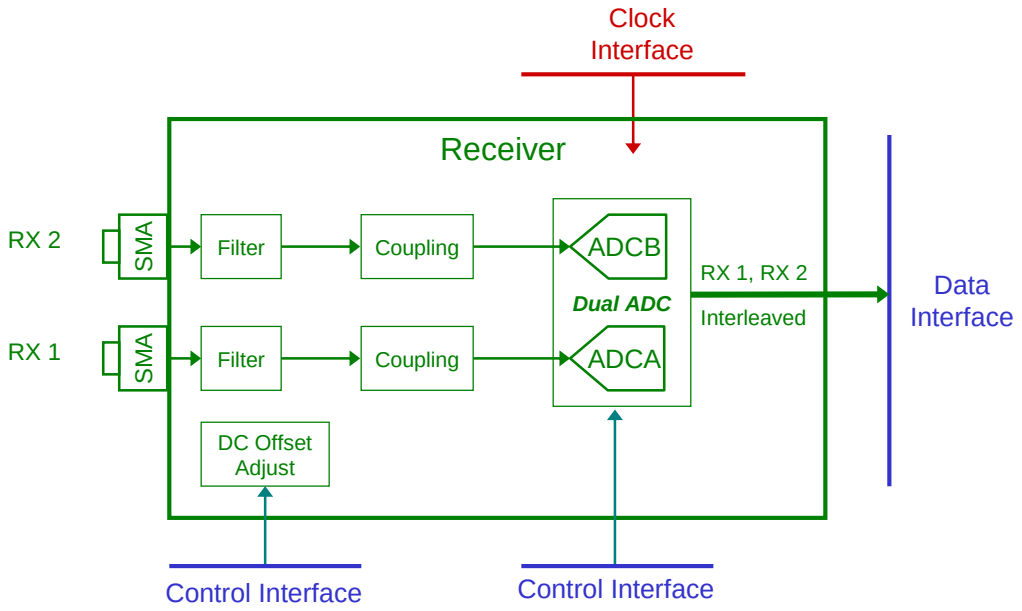


Figure 2-1 Receiver Block Diagram

2.1 Filter Build Option

The Front End Receiver has two filter build options. The standard build bypasses the filter section to provide maximum frequency response. As an option each receiver is designed to accommodate a 3-pole lumped element single ended Butterworth or Chebyshev lowpass filter. Table 2-1 provides a summary of the filter build option parameters. The filter is located at the receiver input prior to coupling and is useful for limiting broadband noise and harmonic distortion entering the ADC. The default build bypasses the input filter section.

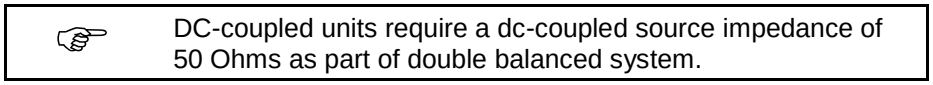
Table 2-1 Lowpass Filter Build Option Parameters

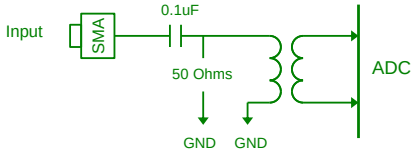
Parameter	Value
Filter Type	Chebyshev or Butterworth
Number of Poles	3
3 dB Bandwidth (Cutoff)	10 to 325 MHz
Passband Ripple (Chebyshev)	0.1 dB standard

2.2 Coupling

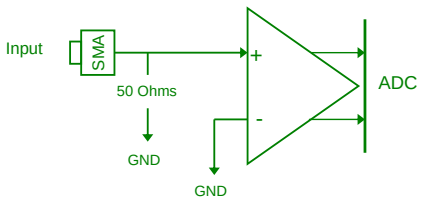
The receiver is available AC or DC coupled as a build option as shown in Figure 2-2. AC coupled units typically offer better high frequency performance and SNR at the expense of low frequency operation. DC-coupled units provide for good mid/low frequency operation down to DC with the expense of added noise and distortion from the coupling amplifier.

AC units block DC signal content with a 0.1 uF series capacitor and are transformer coupled to the ADC. DC-coupled units use a differential amplifier to couple the input signal to the ADC. The differential amplifier also provides signal gain allowing unit operation with a lower input signal amplitude range. DC-coupled units require a dc-coupled system source impedance of 50 Ohms to ensure proper coupling amplifier bias. Other source impedances are supported as a build option.


DC-coupled units require a dc-coupled source impedance of 50 Ohms as part of double balanced system.



AC-Coupled Build Option



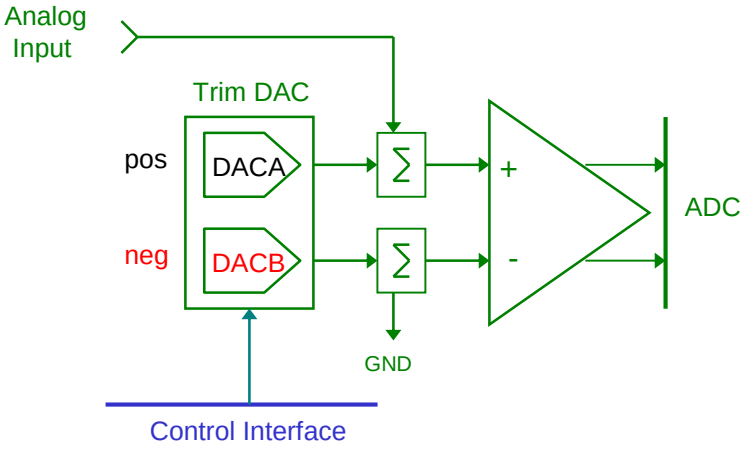
DC-Coupled Build Option

Figure 2-2 Coupling Options (equivalent circuits)

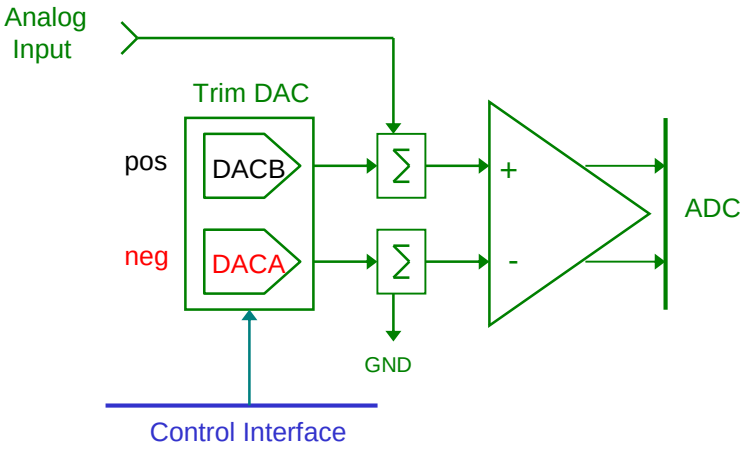
2.3 DC Offset Adjustment (DC-Coupled units only)

The DC-coupled receiver option contains a set of DACs to trim larger DC offset errors that are induced by the coupling amplifier and system DC mismatch. A block diagram of the trim DAC structure is shown in Figure 2-3. The DC offset trimming function is implemented using a dual DAC in a push-pull configuration. The polarity control for the offset is different between channel 1 and 2 due to layout constraints. In channel 1 trim DAC A controls positive offset while DAC B controls negative offset. Channel 2 has the opposite structure. DAC B offsets the ADC input voltage in a positive direction while DAC A offsets the ADC input in a negative direction. Trim DAC register settings can be found in the device data sheet listed in section 5.0. The receiver trim DACs are accessed through the Control Interface via a SPI bus as shown in Figure 2-4.

Only one of the pair of offset trim DACs per input should be active at a time. The unused trim DAC should be set to 0 V.



Channel 1 DC Offset Adjustment



Channel 2 DC Offset Adjustment

Figure 2-3 Trim DAC Operation in DC-Coupled Build Option

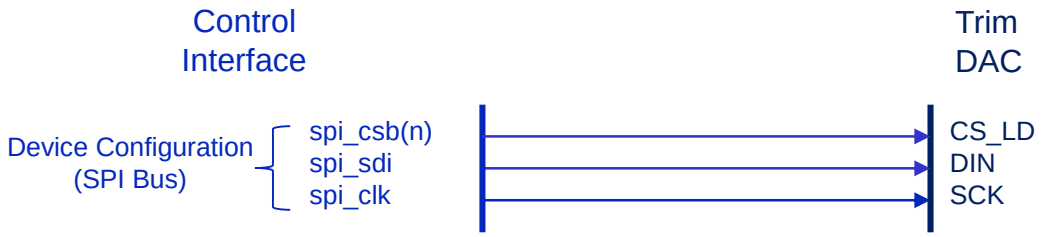


Figure 2-4 Trim DAC Control

2.4 ADC Configuration

The receiver ADC has a number of configuration options available to support different modes of operation. The following sections describe the physical connection of the device in terms of hardwired board connections, clock inputs and control/data interfaces accessible to the user. Operational modes are described in the ADC device data sheet listed in section 5.0. .

2.4.1 ADC Hardware Interface

Selected ADC component physical pin connections are shown in Figure 2-5. The figure shows logical connection of the RX channel interface and individual discrete control pins described in the device data sheet listed in section 5.0.

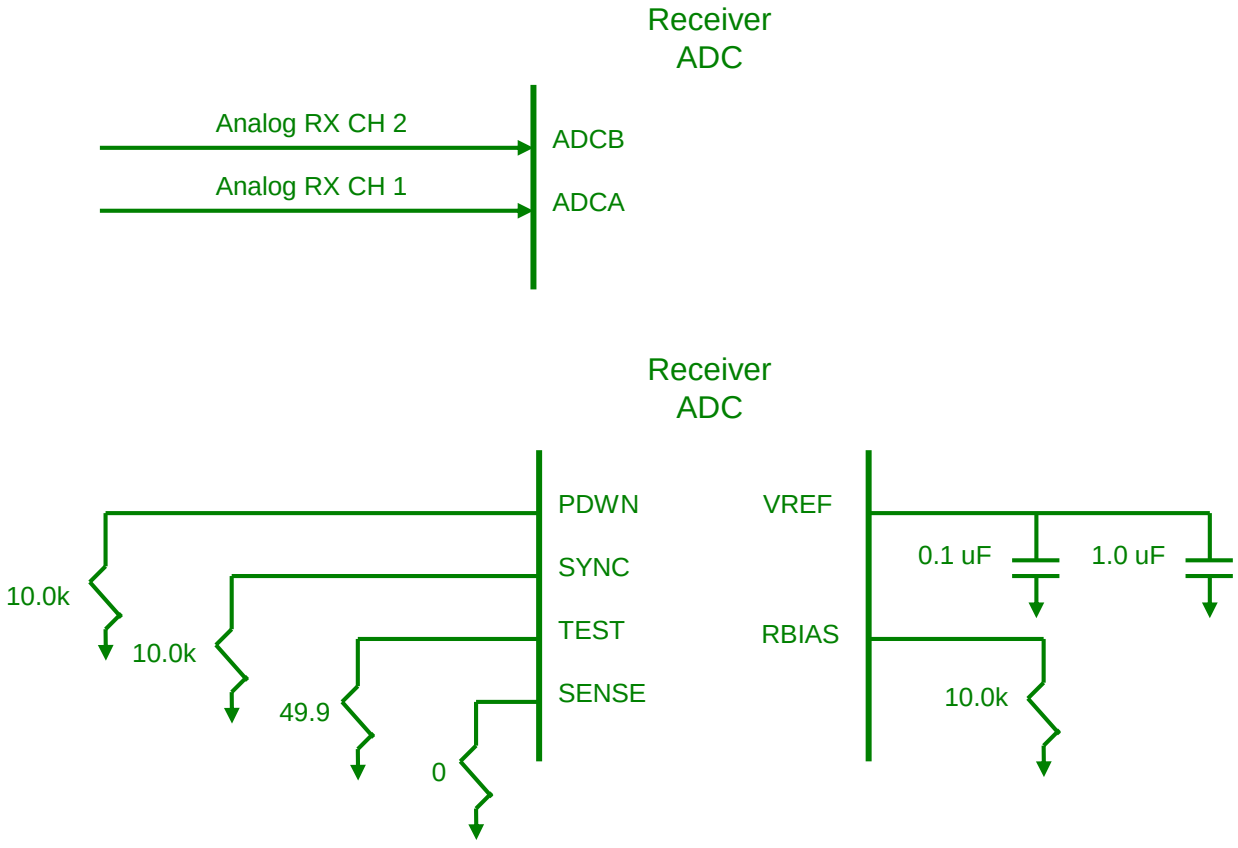


Figure 2-5 Selected RX ADC Physical Connections

2.4.1 ADC Control Interface

A diagram of the ADC control interface is shown in Figure 2-6. The user has access to the ADC command and status registers through the control interface SPI port. A list and description of ADC command and status registers can be found in the device data sheet listed in section 5.0.

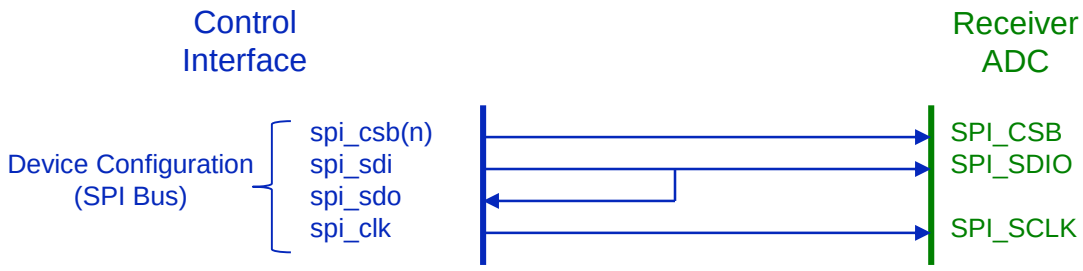


Figure 2-6 ADC Control Interface

2.4.1 ADC Clock Interface

The receiver ADC clock input is sourced by the sample clock distribution network as shown in Figure 2-7.

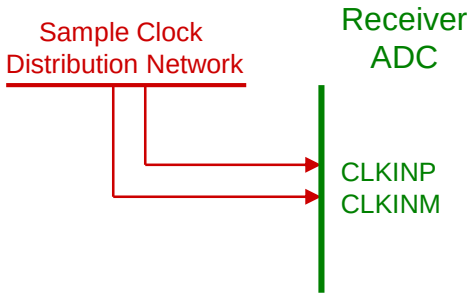


Figure 2-7 ADC Clock Interface

2.4.2 ADC Data Interface

A diagram of the ADC data interface is shown in Figure 2-8. The interface consists of a forwarded LVDS data clock, a 16-bit LVDS interleaved data bus and a single over range LVDS pair. A description of the data transfer protocol can be found in the RX ADC device data sheet listed in section 5.0.

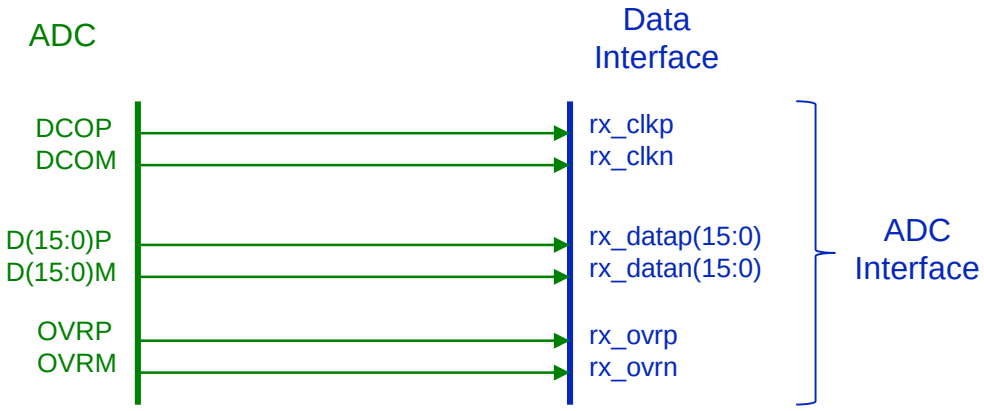


Figure 2-8 ADC Data Interface

3.0 Specifications

The following section lists the performance specifications of the Front End Receiver based on direct unit measurement unless otherwise noted. Measurements are listed as typical and represent the mean performance of a representative sample of units under laboratory conditions as listed in Table 3-1. More information on test setup can be found in section 4.3. Some variation in performance will occur based on build variation, external system performance and environment. See key component device data sheets in section 5.0 for more insight on performance variation.

Table 3-1 Test Environment

Item	Description
Host	Personal Computer, On carrier in PCIe x8 Slot
Air Temperature	25 C (Room)
Cooling	Convection (Fan)
Voltage	Nominal “Typical” levels
ADC Control	Default API from Red Rapids website.
Clock	310 MHz External Clock

3.1 Input Levels

Parameter	Min	Typ	Max	Unit
Input Impedance		50		Ohms
ADC Offset Error(1)	-10	+/-1.5	+10	mV
DC Coupling Offset Error(1)	-50		+50	mV
DC-Coupled Option – DC Offset Control(2)				
Range (at input)	-0.5		0.5	V
Resolution (per step)		500		uV
Full Scale Input (0 dBFS, 20 MHz, 50 ohms)				
AC-Coupled				
Input Voltage		2.5		Vpp
Input Power		+12.0		dBm
DC-Coupled				
Input Voltage		1.0		Vpp
Input Power		+4.0		dBm

Notes: (1) ADC offset dominates when AC coupled; DC coupling circuit offset dominates when DC coupled.
(2) DC offset adjustment is discussed in section 2.3.

3.2 Performance

> ☞ Performance may vary depending on the quality of the power supply and EMI environment of the host.

3.2.1 AC-Coupled Performance

Parameter	Min	Typ	Max	Unit
Passband [1]				
1 dB	1		150	MHz
3 dB	0.1		400	MHz
SNR				
20.17 MHz Input		74.9		dBFS
70.17 MHz Input[2]		74.1		dBFS
125.17 MHz Input [3]		71.1		dBFS
SINAD				
20.17 MHz Input		74.8		dBFS
70.17 MHz Input[2]		74.1		dBFS
125.17 MHz Input[3]		71.0		dBFS
SFDR				
20.17 MHz Input		95		dBc
70.17 MHz Input[2]		89		dBc
125.17 MHz Input [3]		87		dBc
Channel to Channel Isolation				
25 MHz		>90		dB
50 MHz		85		dB
75 MHz		84		dB
100 MHz		81		dB

Notes:
[1] Measured across band using ADC output.
[2] Performance extrapolated from -4.8 dBFS plot due to test equipment limitations.
[3] Performance extrapolated from -2.0 dBFS plot due to test equipment limitations.

3.2.2 DC-Coupled Performance

Parameter	Min	Typ	Max	Unit
Passband [1]				
1 dB	DC		200	MHz
3 dB	DC		450	MHz
SNR				
20.17 MHz Input		67.7		dBFS
70.17 MHz Input		66.7		dBFS
125.17 MHz Input		65.0		dBFS
SINAD				
20.17 MHz Input		67.6		dBFS
70.17 MHz Input		66.6		dBFS
125.17 MHz Input		59.0		dBFS
SFDR				
20.17 MHz Input		93		dBc
70.17 MHz Input		82		dBc
125.17 MHz Input		61		dBc
Channel to Channel Isolation				
1 MHz		>100		dB
50 MHz		87		dB
100 MHz		81		dB
150 MHz		75		dB
200 MHz		72		dB

Notes:
[1]Measured across band using ADC output.

3.3 Absolute Maximums

Stresses above those listed in Table 3-2 may cause damage to the unit. The operation of the unit at these or any other conditions outside of those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may degrade unit reliability.

Table 3-2 Absolute Maximum Specifications

Parameter	Min	Typ	Max	Unit
Receiver Inputs (50 Ohms)				
AC-Coupled				
DC Input Voltage	-10		10	V
AC Voltage Swing			5	Vpp
AC Input Power			+18	dBm
DC-Coupled				
DC Input Offset plus AC swing	-3		3	V
AC Voltage Swing (Centered at 0V)			5	Vpp
AC Input Power (Centered at 0V)			+18	dBm

! Exposure to absolute maximum conditions for extended periods may degrade unit reliability.

4.0 Typical Performance Characteristics

The following sections contain spectrum plots of the receiver showing typical performance for a variety of sine wave inputs. The receiver performance section is divided into AC and DC coupled subsections. Each sine input is characterized using a 32k point FFT.

4.1 AC-Coupled

The following receiver plots were taken with the receiver configured for the AC-coupled build option with the input filter bypassed.

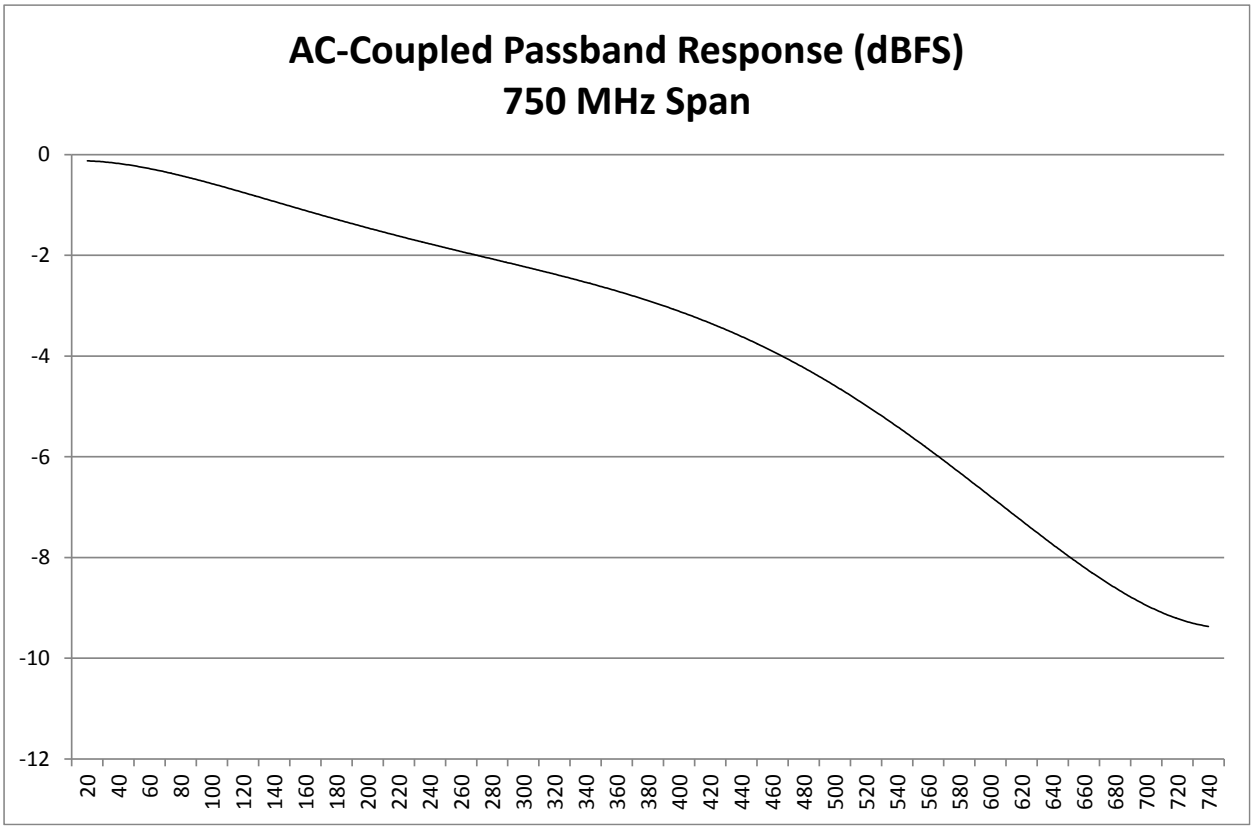


Figure 4-1 AC-Coupled Passband Profile 1 MHz to 750 MHz

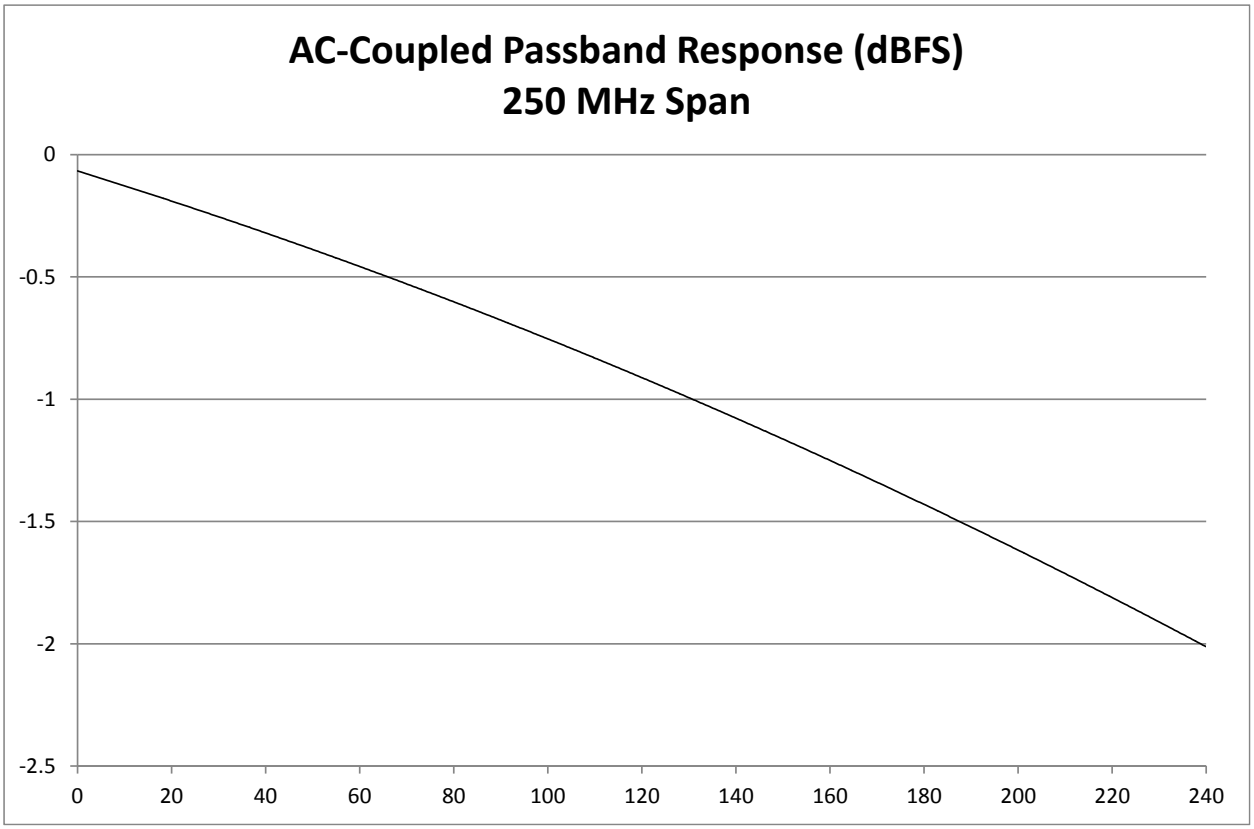


Figure 4-2 AC-Coupled Passband Profile 1 MHz to 300 MHz

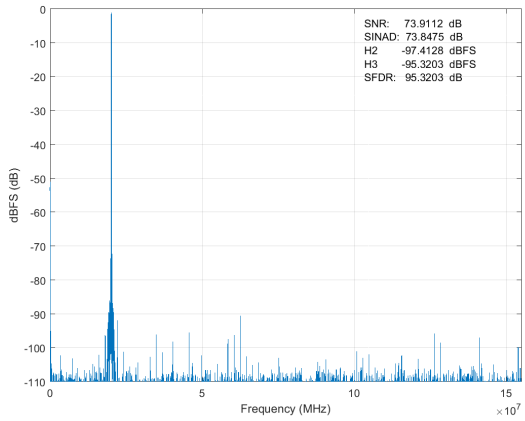


Figure 4-3 20.17 MHz, -1.0dBFS,

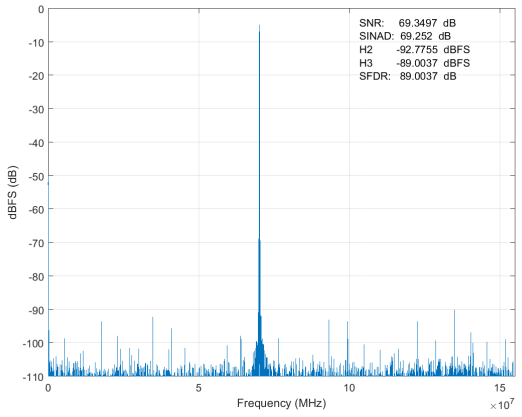


Figure 4-4 70.17 MHz, -4.8 dBFS,

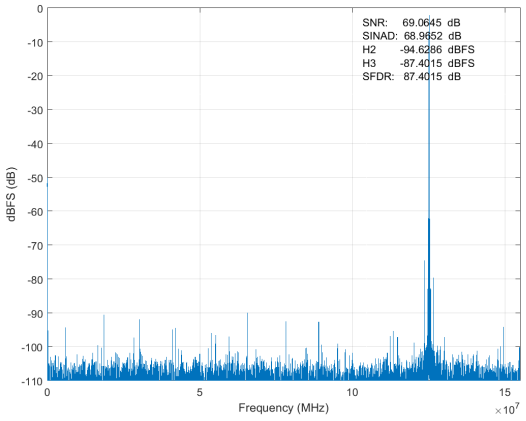


Figure 4-5 125.17 MHz, -2.0dBFS

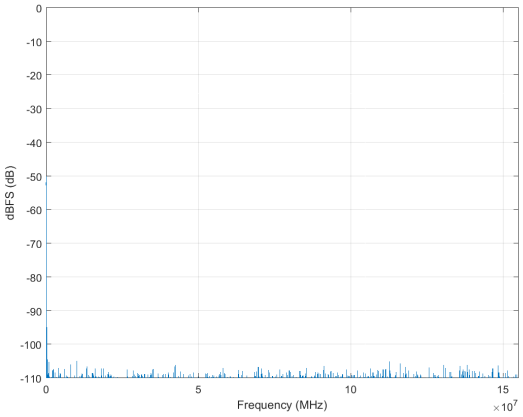


Figure 4-6 Terminated Input

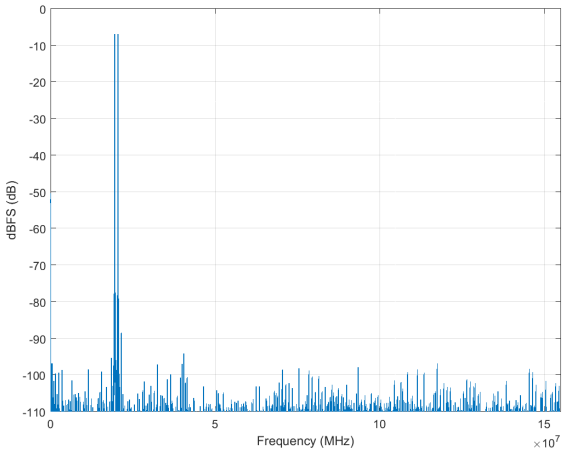


Figure 4-7 Two-tones 19.5 and 20.5 MHz at -7dBFS

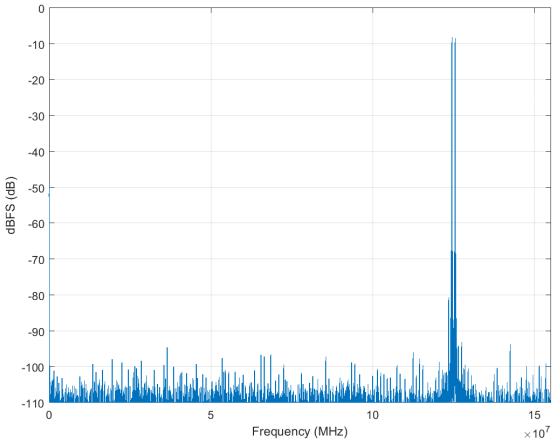


Figure 4-8 Two-tones 124.5 and 125.5 MHz at -8dBFS

4.2 DC-Coupled

The following receiver plots were taken with the receiver configured for the DC-coupled build option with the input filter bypassed.

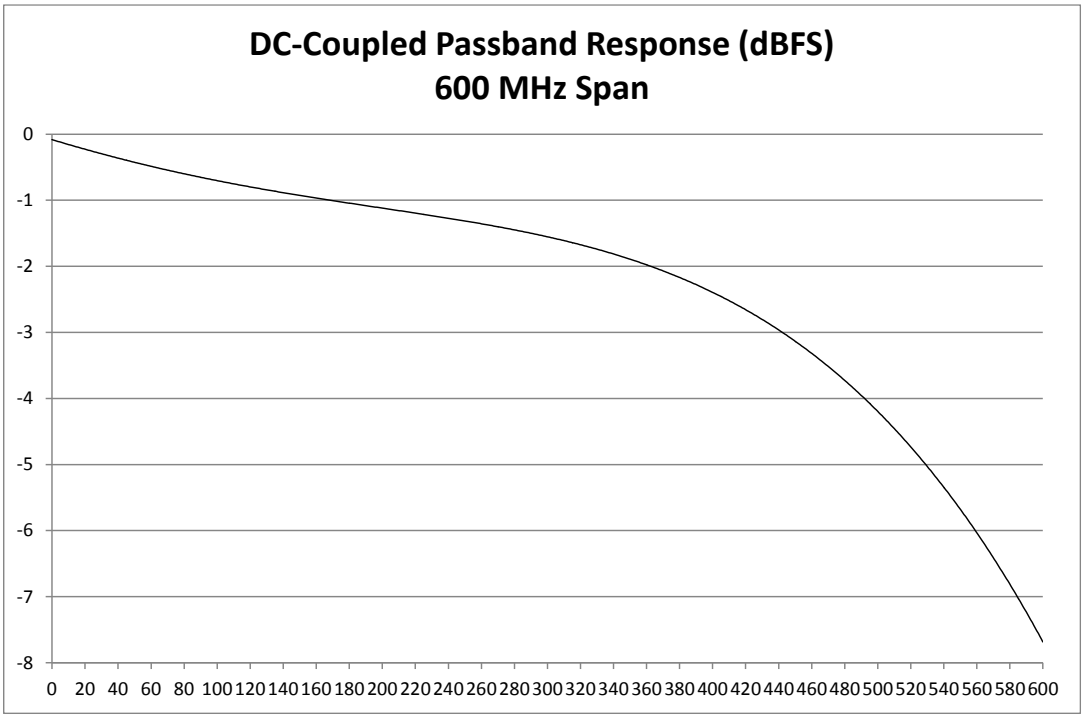


Figure 4-9 DC-Coupled Passband Profile DC to 600 MHz

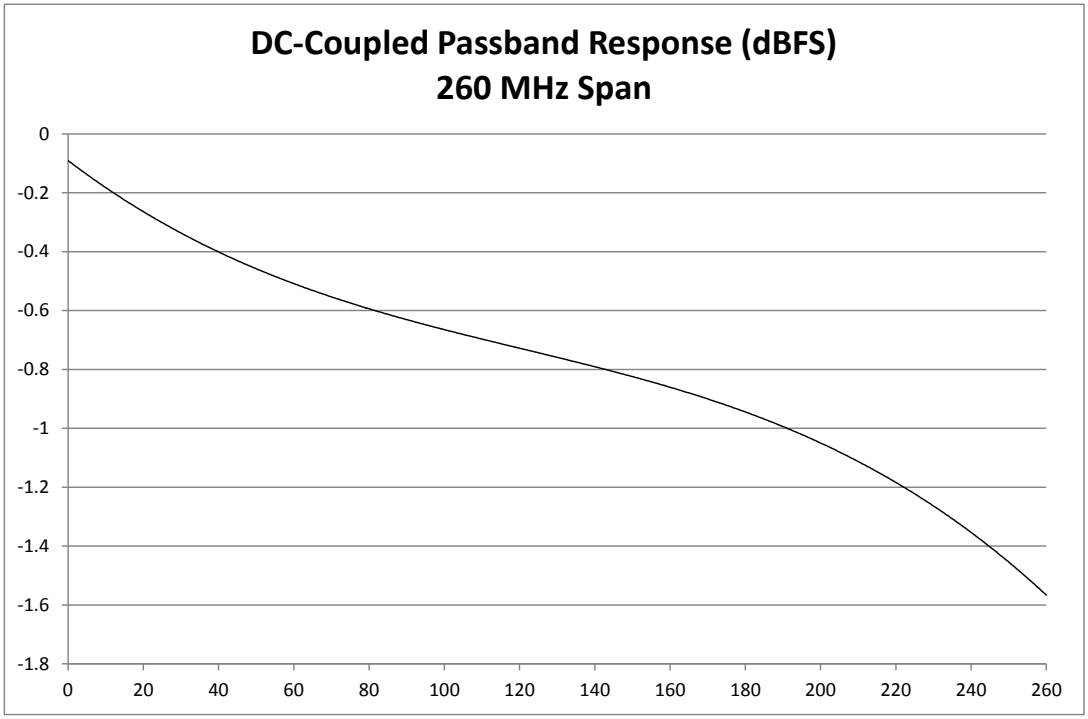


Figure 4-10 DC-Coupled Passband Profile DC to 260 MHz

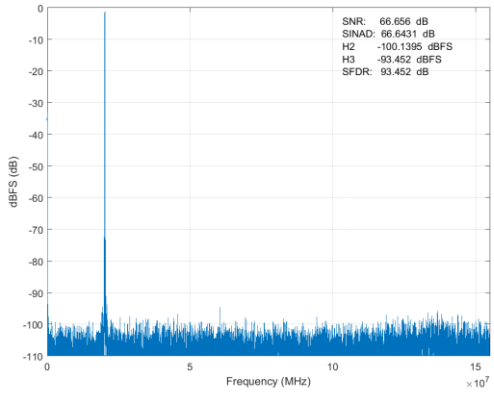


Figure 4-11 20.17 MHz, -1 dBFS,

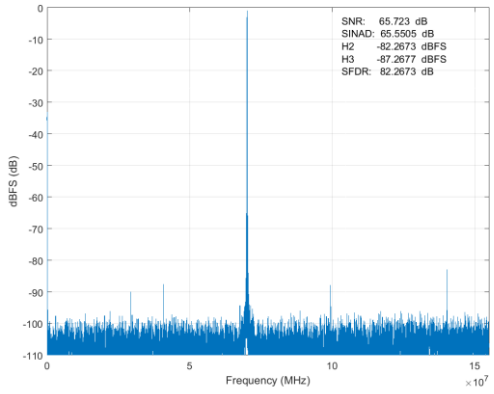


Figure 4-12 70.17 MHz, -1 dBFS,

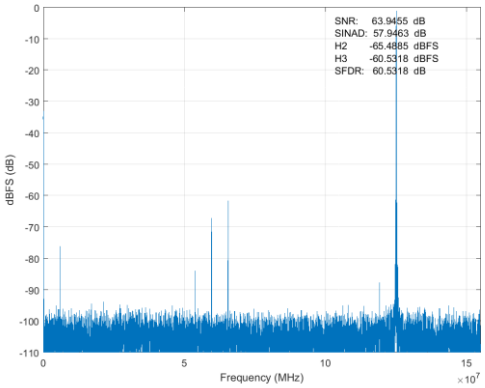


Figure 4-13 125.17 MHz, -1dBFS

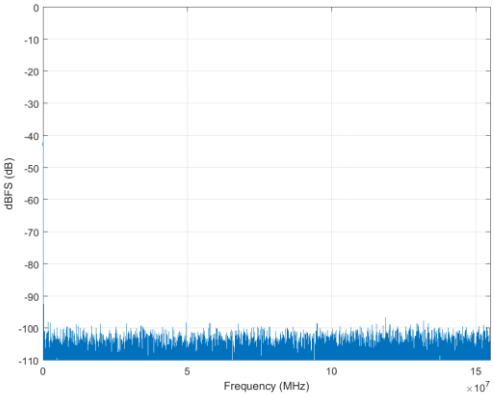


Figure 4-14 Terminated Input

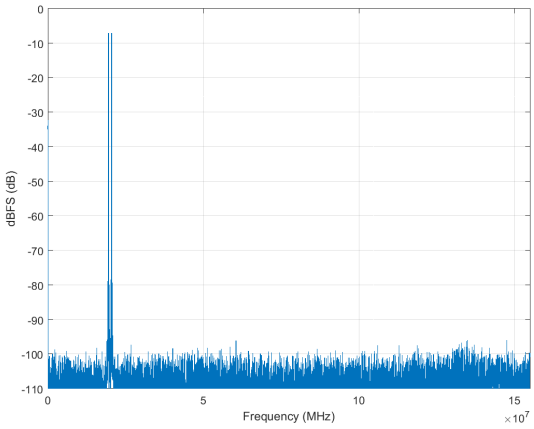


Figure 4-15 Two-tones 19.5 and 20.5 MHz at -7dBFS

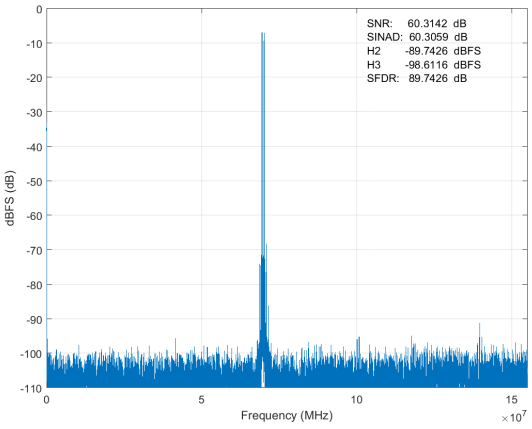


Figure 4-16 Two-tones 69.5 and 70.5 MHz at -7dBFS

4.3 Generating Characterization Plots

The wide dynamic range and input bandwidth characteristics of the receiver levy strict signal conditioning requirements on test equipment used to characterize board performance. Even the highest quality general purpose RF signal generators output harmonics and noise that must be reduced in order to accurately characterize system performance. Generally a narrow bandpass filter is inserted between the signal generator output and the Adapter Module receiver input. The bandpass filter should be reasonably narrow to eliminate generator harmonics and limit the amount of generator phase noise input into the receiver. Red Rapids' characterization plots were created using 5% bandwidth 7-section Chebyshev filters with > 55 dB of stop band rejection. We used filters from TTE such as their KC7t-70m-3.5m-50-720a. Table 4-1 contains a list of test equipment used to generate the characterization plots of section 4.0. The characterization frequency plots were generated by performing a 32k FFT on 32k data samples collected from the receiver.

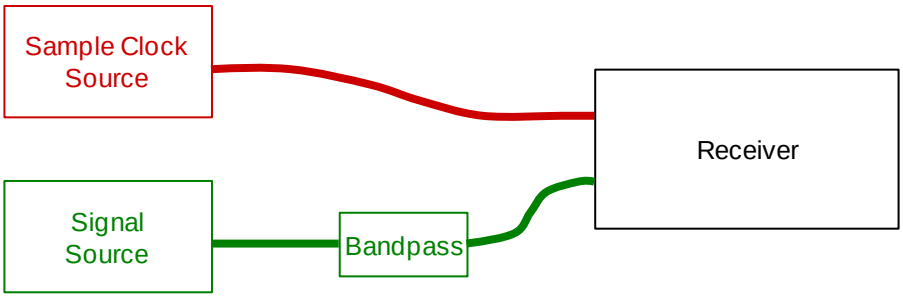


Figure 4-17 Characterization Setup

☞ Use a narrow bandpass filter between the signal generator and receiver card to accurately characterize system.

Table 4-1 Characterization Test Equipment

Function	Part Number	Manufacturer
Sample Clock Source	HP8648B	Agilent
Signal Bandpass Filter (one of several)	KC7t-70m-3.5m-50-720a	TTE
Signal Source	HP8648B	Agilent

5.0 Key Components

Key hardware components for the Receiver are listed in Table 5-1. Device datasheets can be downloaded from vendor websites for more information.

Table 5-1 Key Hardware Components

Component	Part Number	Vendor	Comments
Receiver ADC	AD9652BBCZ-310	Analog Devices	Dual 16-bit 310 Msps A-D Converter
Trim DAC	LTC1661CMS8#PBF	Linear Technology	Dual 10-bit Micropower DAC

6.0 Technical Support

Please feel free to contact us if you have a technical question about or problem with our product. We understand that our customers have tight deadlines and time is of the essence in development and production cycles. We will make every effort to resolve problems as quickly as possible.

Web: www.redrapids.com

Email: support@redrapids.com

Phone: 972-671-9570

Fax: 972-671-9572

Please include the following information with your correspondence:

- Contact Information
- Product Model
- Host Card or System (PC, PCI Carrier, Single Board Computer)
- Operating System
- Problem Description