Front End 000-007
Quad 16-Bit 250 Msps Receiver
Reference Manual

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1.0 Introduction

1.1 Contents and Structure

This manual describes the Front End 000-007 receiver hardware. The focus of this manual is the electrical function of the hardware including control structure, signal flow and key components. The latest product documentation and software is available for download from the Red Rapids web site (www.redrapids.com) by following the Technical Support link.

1.2 Conventions

This manual uses the following conventions:

- Hexadecimal numbers are prefixed by "0x" (e.g. 0x00058C).

☞	Text in this format highlights useful or important information.

!	Text shown in this format is a warning. It describes a situation that could potentially damage your equipment. Please read each warning carefully.

The following are acronyms used in this manual.

- **AC** Alternating Current (Greater than 0 Hertz)
- **ADC** Analog to Digital Converter
- **DAC** Digital to Analog Converter
- **dB** Decibels
- **dBFS** Decibels Relative to Full Scale
- **dBm** Decibels Relative to One milliwatt
- **DC** Direct Current (0 Hertz)
- **FFT** Fast Fourier Transform
- **LVDS** Low Voltage Differential Signaling
- **MHz** Megahertz
- **mV** millivolts
- **MSPS** Mega Samples per Second
- **PGA** Programmable Gain Amplifier
- **RF** Radio Frequency
- **SFDR** Spur Free Dynamic Range
- **SINAD** Signal-to-Noise and Distortion Ratio
- **SNR** Signal-to-Noise Ratio
- **Vpp** Voltage, peak-to-peak

1.3 Revision History

Version	Date	Description
R00	12/11/2013	Initial release.
R01	08/05/2014	
R02	12/6/2016	Removed DC-Coupled References

2.0 Description

The Front End 000-007 receiver is a high performance quad-channel structure built around the Texas Instruments ADS42LB69 dual 16-bit 250 Msps ADC.

Features[1]:

- Quad Channel
- 16-bit Architecture
- SNR (fin = 20 MHz) 74.8 dB (2.5 Vpp), 73.5 dB (2.0 Vpp)
- SFDR (fin = 20 MHz) 87 dBc (2.5 Vpp), 90 dBc (2.0 Vpp)
- Sample Rate up to 250 Msps
- 5-Pole Chebyshev or Butterworth lowpass input filter (optional)
- 500 MHz 3dB Bandwidth
- AC Coupled

Note [1]: Features listed are mode and build dependent. See specifications and performance sections for more information.

A block diagram of the Front End 000-007 receiver is shown in Figure 2-1. The receiver consists of four independent analog input channels labeled 1 through 4. A single receiver channel consists of a front panel SMA connector, an optional signal conditioning filter, an AC coupling mechanism and an ADC. Each analog input is digitized by an ADC to create data samples that stream to the user interface under the timing control of a high-speed precision clock distributed through a low noise network. The following paragraphs provide details about each element of the receiver section.

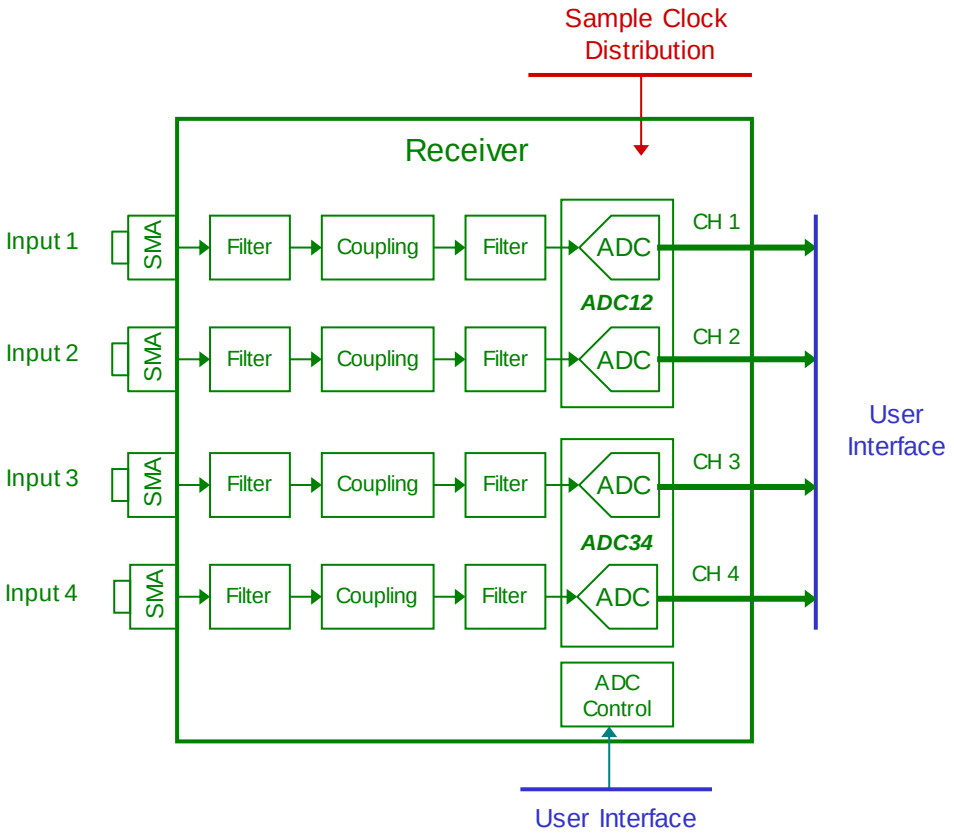


Figure 2-1 Receiver Block Diagram

2.1 Filter Build Option

The Front End Receiver has two filter build options. The standard build bypasses the filter section to provide maximum frequency response. Table 2-1 provides a summary of the populated filter build option parameters. The following paragraph provides a brief description of the filter options.

Table 2-1 Lowpass Filter Build Option Parameters

Parameter	Value
Filter Type	Chebyshev or Butterworth
Number of Poles	5
3 dB Bandwidth (Cutoff)	10 to 325 MHz
Passband Ripple (Chebyshev)	0.1 dB standard

The receiver is designed to accommodate a 5-pole lumped element single ended Butterworth or Chebyshev lowpass filter as a build option. The filter is located at the receiver input prior to coupling and is useful for limiting broadband noise and harmonic distortion entering the ADC. The default build bypasses the input filter section.

2.2 Coupling

The receiver is AC coupled as shown in Figure 2-2. AC coupled units typically offer better high frequency performance and SNR at the expense of low frequency operation. AC units block DC signal content with a 0.1 uF series capacitor and are transformer coupled to the ADC.

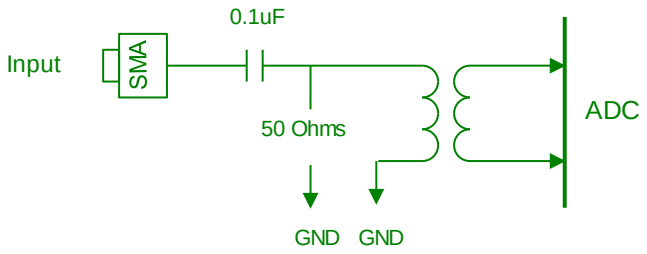


Figure 2-2 Coupling Option (equivalent circuit)

2.3 ADC Configuration

The receiver ADC has a number of configuration options available to support different modes of operation. These operational modes are described in the ADC device data sheet listed in section 5.0. Some features are user configurable via the ADC SPI port. Some features are hardwired in the board design. The following paragraphs describe how the ADC device is connected for use in Front End 000-007.

Front End 000-007 has four receiver channels routed to two dual ADCs labeled as ADC12 and ADC34 with RX channels 1 and 2 routed to ADC12 and RX channels 3 and 4 routed to ADC34. A generic block diagram of the RX channel configuration is shown in Figure 2-3. Each ADC is programmed independently using the SPI port through the user interface.

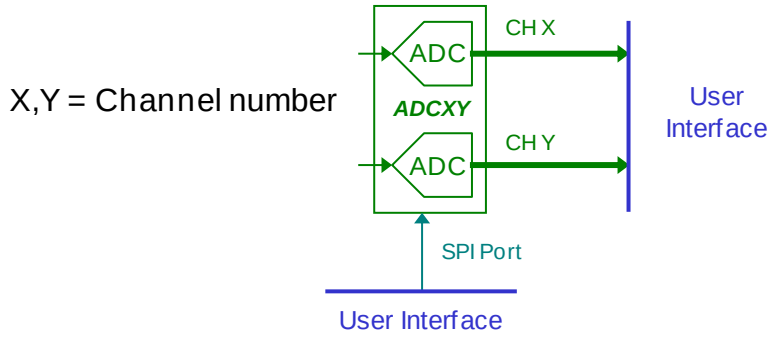


Figure 2-3 ADC RX Channel Configuration

A summary of the ADC device hardware configuration is provided in Table 2-2. This table describes ADC device control pin physical connections. Pin names are taken from the device data sheet listed in section 5.0.

Table 2-2 Receiver ADC Device Configuration

Device Pin Name	Connection	Description
INAP/M	RX CH1 input RX CH3 input	Analog input 1 (ADC12) Analog Input 3 (ADC34)
INBP/M	RX CH2 input RX Ch4 input	Analog input 2 (ADC12) Analog Input 4 (ADC34)
VCM	Analog Input Bias	Used to bias analog inputs for ADC
CLKINP/M	Sample Clock	Connected to sample clock distribution network
SYNCINP SYNCINM	Pull down Pull up	10.0k Ohm to ground. (not used) 10.0k Ohm to Va (supply)
RESET	PCI Reset	Connected to PCI system reset

Table 2-3 provides a list of ADC user interface connections. These are connections between the ADC and the user interface that provide access to ADC control options and data.

Table 2-3 ADC User Interface Connections

Device Pin Name	User Interface Name	Description
SEN	spi_csb(n)	SPI port chip select (one each for ADC12 and ADC34)
SDATA	spi_sdi	SPI port data in
SCLK	spi_clk	SPI port clock
SDOUT	spi_sdo	SPI port data out
CLOCKOUTP/M	RX1_CLKP/N RX3_CLKP/N	RX1_CLK is from ADC12 RX3_CLK is from ADC34
DA(14:0)P/M	RX1_DATAP/N(7:0), RX3_DATAP/N(7:0)	RX1_DATA from ADC12 RX3_DATA from ADC34
DB(14:0)P/M	RX2_DATAP/N(7:0), RX4_DATAP/N(7:0)	RX2_DATA from ADC12 RX4_DATA from ADC34
CTRL1	CH1, 3 OVR	Over range flag for CH1 (ADC12) CH3 (ADC34)
CTRL2	CH2, 4 OVR	Over range flag for CH2 (ADC12) CH4 (ADC34)

2.3.1 ADC User Control Interface

A diagram of ADC user control interface is shown in Figure 2-4. The user has access to the ADC command and status registers through a SPI port. In addition there are discrete control and status lines that are available to the user through the User Interface.

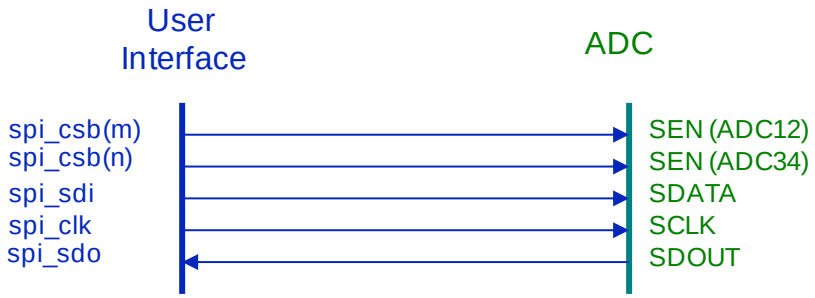
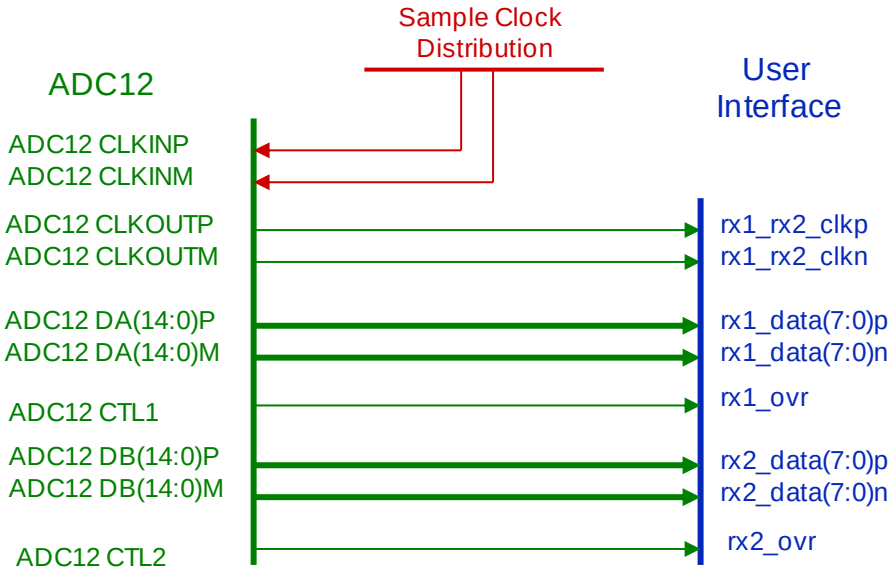


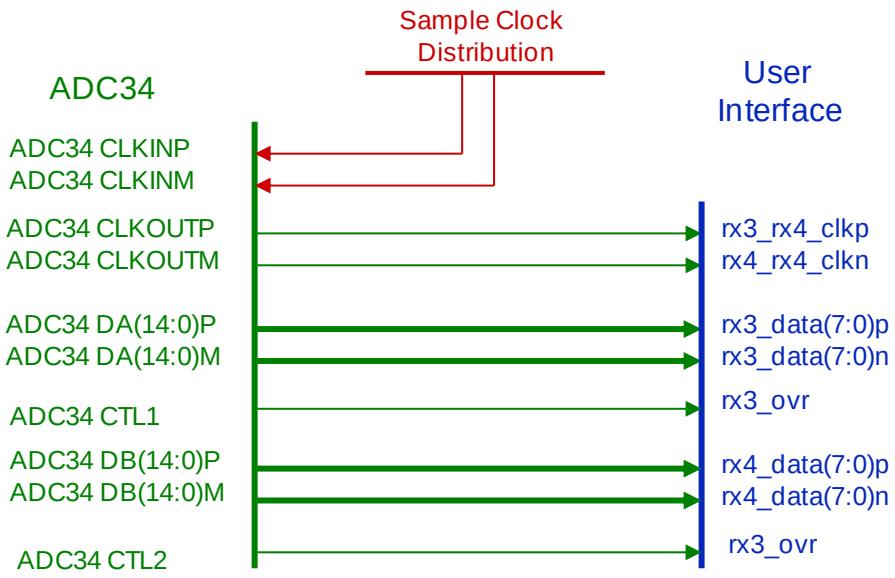
Figure 2-4 ADC User Control Interface

2.3.2 ADC User Data Interface

A diagram of the ADC user data interface is shown in Figure 2-5. Each ADC digital data output encodes 2 bits per clock period with even bits output on the rising edge of clock and odd bits on the falling edge. In this manner 16 bits of data are transferred over 8 LVDS pairs. The ADC outputs a forwarded data clock. Please see the ADC datasheet referenced in section 5.0 for more information on data transfer.



ADC12 User Interface (Channel 1 and Channel 2)



ADC34 User Interface (Channel 3 and Channel 4)

Figure 2-5 ADC User Data Interface

3.0 Specifications

The following section lists the performance specifications of the Front End Receiver based on direct unit measurement unless otherwise noted. Measurements are listed as typical and represent the mean performance of a representative sample of units under laboratory conditions as listed in Table 3-1. More information on test setup can be found in section 0. Some variation in performance will occur based on build variation, external system performance and environment. See key component device data sheets in section 5.0 for more insight on performance variation.

Table 3-1 Test Environment

Item	Description
Host	Personal Computer, On carrier in PCIe x4 Slot
Air Temperature	25 C (Room)
Cooling	Convection (Fan)
Voltage	Nominal “Typical” levels
Clock	250 MHz External Clock

3.1 Input Levels

Parameter	Min	Typ	Max	Unit
Input Impedance		50		Ohms
ADC Offset Error[1]	-20		+20	mV
ADC Gain Error	-5%		+2%	FS
Full Scale Input (0 dBFS, 50 ohms) [2]				
2.0 Vpp mode				
Input Voltage		2.2		Vpp
Input Power		+10.8		dBm
2.5 Vpp mode				
Input Voltage		+2.8		Vpp
Input Power		+12.8		dBm

Notes: [1] ADC offset dominates when AC coupled
[2] Average full scale power input across first Nyquist zone (125 MHz).

3.2 Performance

> ☞ Performance may vary depending on the quality of the power supply and EMI environment of the host.

Parameter	Min	Typ	Max	Unit
Passband [1]				
1 dB	1		250	MHz
3 dB	0.1		500	MHz
SNR[2]				
2.0 Vpp mode				
20.17 MHz Input		73.5		dB
70.17 MHz Input		72.5		dB
124.17 MHz Input		71.4		dB
2.5 Vpp mode				
20.17 MHz Input		74.8		dB
70.17 MHz Input		73.4		dB
124.17 MHz Input		72.3		dB
SINAD[2]				
2.0 Vpp mode				
20.17 MHz Input		73.4		dB
70.17 MHz Input		72.4		dB
124.17 MHz Input		71.3		dB
2.5 Vpp mode				
20.17 MHz Input		74.7		dB
70.17 MHz Input		73.3		dB
124.17 MHz Input		72.2		dB
SFDR				
2.0 Vpp mode				
20.17 MHz Input[3]		90		dBc
70.17 MHz Input[4]		86		dBc
124.17 MHz Input[5]		80		dBc
2.5 Vpp mode				
20.17 MHz Input[3]		87		dBc
70.17 MHz Input[4]		86		dBc
124.17 MHz Input[5]		80		dBc
Channel to Channel Isolation				
50 MHz		90		dB
250 MHz		73		dB
500 MHz		72		dB

Notes:
[1] Measured across band using ADC output.
[2] Performance extrapolated from -11 dBFS measurements due to test equipment limitations (filter bleed through).
[3] Derived from -1.1 dBFS measurements due to test equipment limitations.
[4] Derived from -6.0 dBFS measurements due to test equipment limitations.
[5] Derived from -3.0 dBFS measurements due to test equipment limitations.

3.3 Absolute Maximums

Stresses above those listed in Table 3-2 may cause damage to the unit. The operation of the unit at these or any other conditions outside of those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may degrade unit reliability.

Table 3-2 Absolute Maximum Specifications

Parameter	Min	Typ	Max	Unit
Receiver Inputs (50 Ohms)				
DC Input Voltage	-10		10	V
AC Voltage Swing			4.4	Vpp
AC Input Power			+17	dBm

> **!** Exposure to absolute maximum conditions for extended periods may degrade unit reliability.

4.0 Typical Performance Characteristics

The following sections contain spectrum plots of the receiver showing typical performance for a variety of sine wave inputs. Each sine input is characterized using a 32k point FFT.

4.1 Receiver Performance

The following receiver plots were taken with the receiver configured for the AC-coupled build option with the input filter bypassed.

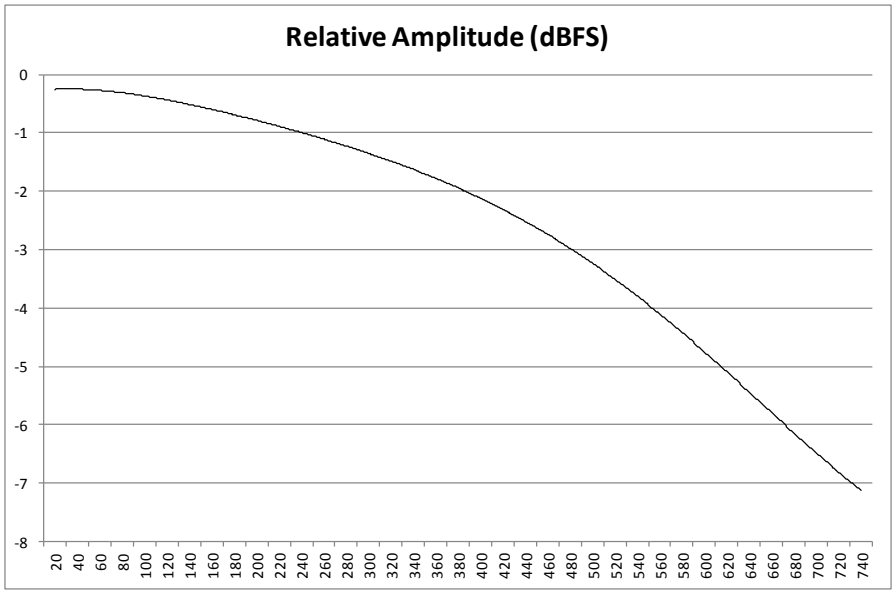


Figure 4-1 AC-Coupled Passband Profile 1 MHz to 750 MHz

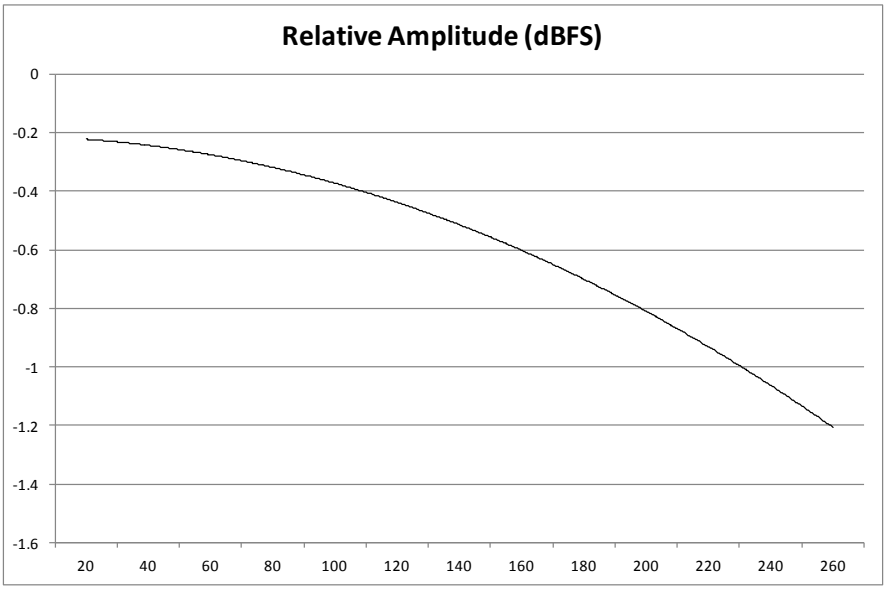


Figure 4-2 AC-Coupled Passband Profile 1 MHz to 250 MHz

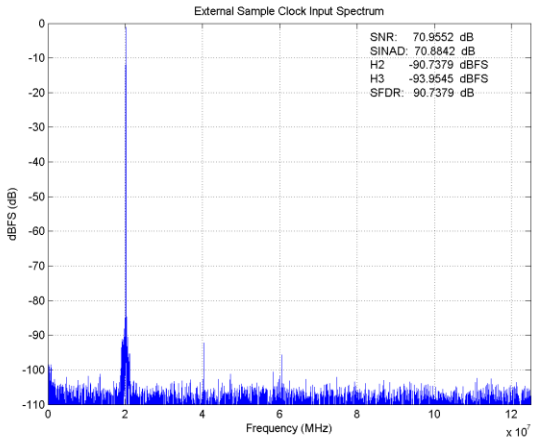


Figure 4-3 20.17357MHz, -1.1dBFS,

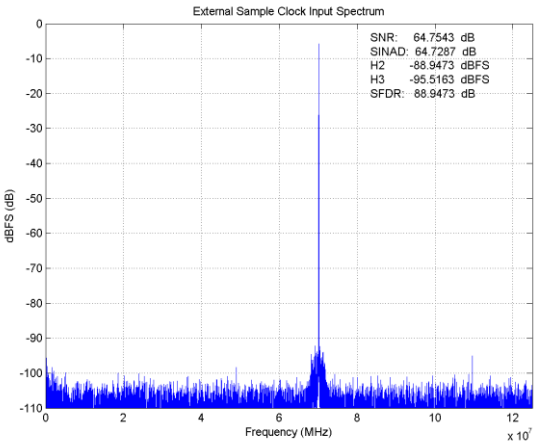


Figure 4-4 70.17347MHz, -6.0 dBFS,

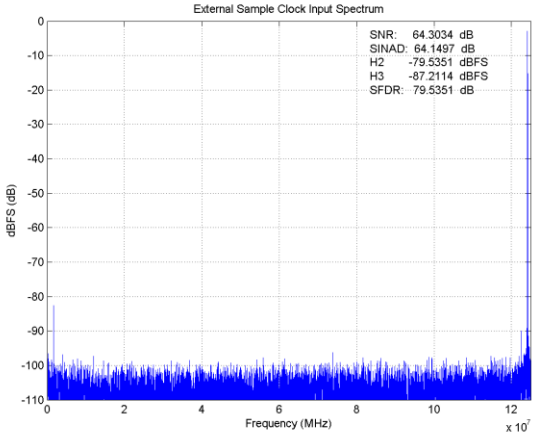


Figure 4-5 124.17357MHz, -3.0dBFS

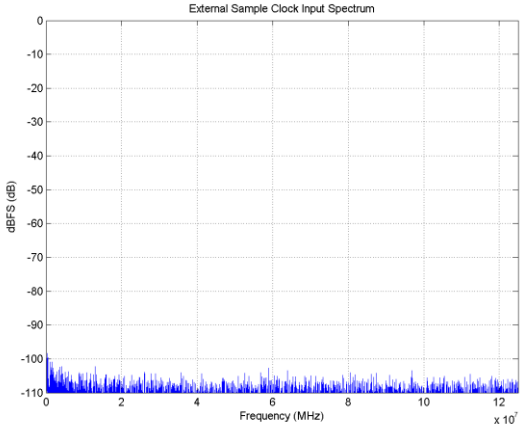


Figure 4-6 Terminated Input

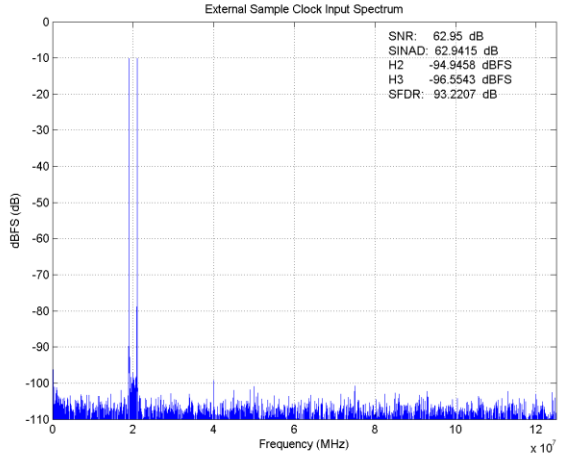


Figure 4-7 Two-tones 19 and 21 MHz at -10 dBFs

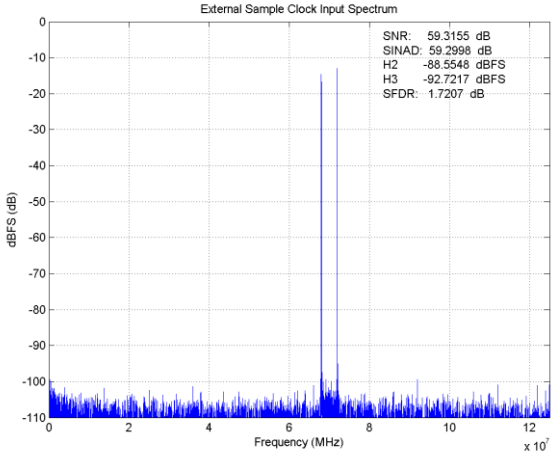


Figure 4-8 Two-tones 68 and 72 MHz at -13 dBFs

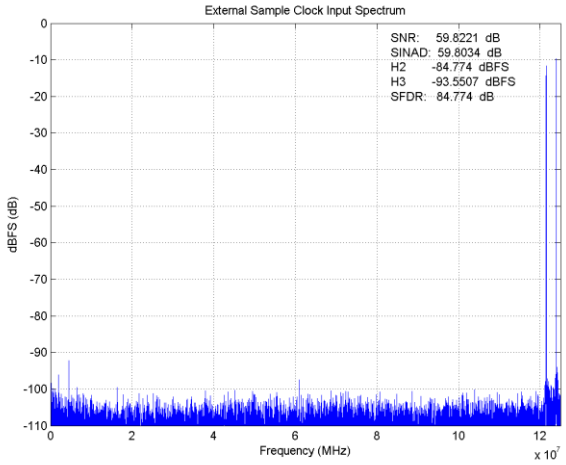


Figure 4-9 Two-tones 121.5 and 124 MHz at -10 dBFs

4.2 Generating Characterization Plots

The wide dynamic range and input bandwidth characteristics of the receiver levy strict signal conditioning requirements on test equipment used to characterize board performance. Even the highest quality general purpose RF signal generators output harmonics and noise that must be reduced in order to accurately characterize system performance. Generally a narrow bandpass filter is inserted between the signal generator output and the Adapter Module receiver input. The bandpass filter should be reasonably narrow to eliminate generator harmonics and limit the amount of generator phase noise input into the receiver. Red Rapids' characterization plots were created using 5% bandwidth 7-section Chebyshev filters with > 55 dB of stop band rejection. We used filters from TTE such as their KC7t-70m-3.5m-50-720a. Table 4-1 contains a list of test equipment used to generate the characterization plots of section 4.0. The characterization frequency plots were generated by performing a 32k FFT on 32k data samples collected from the receiver.

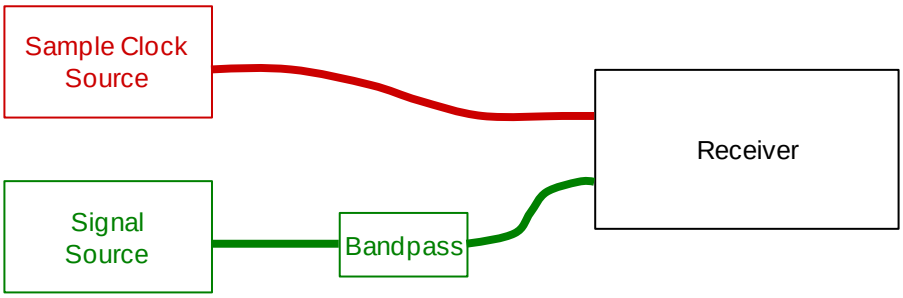


Figure 4-10 Characterization Setup

☞ Use a narrow bandpass filter between the signal generator and receiver card to accurately characterize system.

Table 4-1 Characterization Test Equipment

Function	Part Number	Manufacturer
Sample Clock Source	HP8648B	Agilent
Signal Bandpass Filter (one of several)	KC7t-70m-3.5m-50-720a	TTE
Signal Source	HP8648B	Agilent

5.0 Key Components

Key hardware components for the Receiver are listed in Table 5-1. Device datasheets can be downloaded from vendor websites for more information.

Table 5-1 Key Hardware Components

Component	Part Number	Vendor	Comments
Receiver ADC	ADS42LB69	Texas Instruments	Dual Channel 16-bit, 250 Msps ADC

6.0 Technical Support

Please feel free to contact us if you have a technical question about or problem with our product. We understand that our customers have tight deadlines and time is of the essence in development and production cycles. We will make every effort to resolve problems as quickly as possible.

Web: www.redrapids.com

Email: support@redrapids.com

Phone: 972-671-9570

Fax: 972-671-9572

Please include the following information with your correspondence:

- Contact Information
- Product Model
- Host Card or System (PC, PCI Carrier, Single Board Computer)
- Operating System
- Problem Description