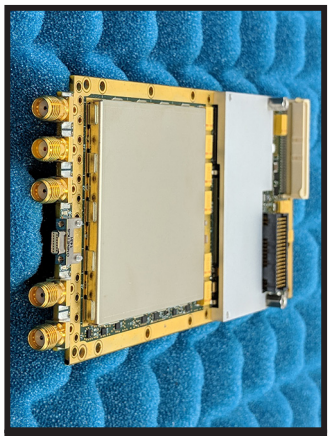
Red Rapids

SigFPGA™ XCVR2 16/310

Model 372

PCIe

XMC



CCXMC

VPX

The SigFPGA™ product family provides the ideal platform to rapidly field application specific signal acquisition and generation functions minus the expense of custom hardware development. All of the products share a common FPGA processing architecture and code base with different interface options tailored to a variety of market needs.

The Model 372 is designed around the Analog Devices AD9652 16-bit dual ADC and AD9142A DAC. The 310 MHz sample clock is supplied by either the on-board frequency synthesizer or an external source. The frequency synthesizer can be phase locked to the local 10 MHz TCXO or an external reference can be used to achieve system-wide phase coherence.

Adopting open architecture hardware and software standards allows SigFPGA™ products to seamlessly transition from the desktop to embedded platforms.

Typical Applications

Radar & comms	Test & measurement
Signal record/playback	Acqusition & telemetry
Software defined radio	Medical diagnostics
Transponder	DSP accelerator

Two AC or DC coupled 16-bit ADC channels

Two AC or DC coupled 16-bit DAC channels

Three Xilinx Kintex-7 FPGA size options

Two banks of optional QDR II+ SRAM

Internal or external sample clock (≤ 310 MHz)

Phase locked frequency synthesizer

Internal or external 10 MHz reference

Temperature and power supply monitors

PCI Express (PCIe) x8 or x4 host bus

High performance scatter-gather DMA

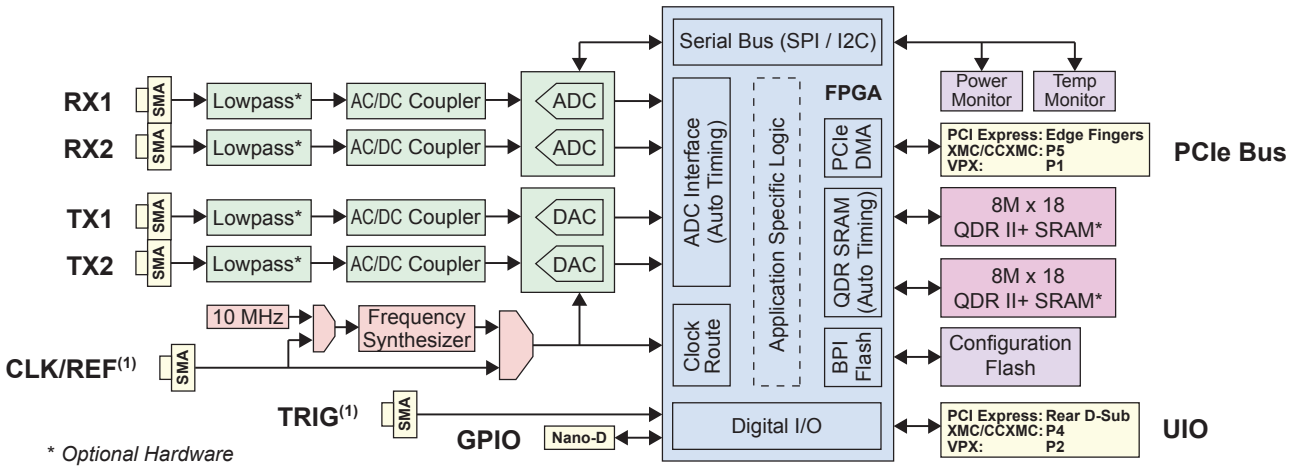
Front and rear auxiliary connectors

Configuration flash loads from JTAG or host

FPGA VHDL core library for data interfaces

FPGA VHDL reference design with source

Demostration software (C) with source



* Optional Hardware

Form Factor

PCI Express (air cooled)	PCI Express 2.1, standard height, half-length, x8 or x4 physical edge connector
XMC (air cooled)	ANSI/VITA 42.0 single-width, ANSI/VITA 42.3
CCXMC (conduction cooled)	XMC plus ANSI/VITA 20
VPX (air or conduction cooled)	3U Eurocard, VITA 65, front panel I/O

FPGA Selection

Device	Xilinx Kintex-7
Size	XC7K160T, XC7K325T, or XC7K410T
Speed/Temperature Grade	-2I (Industrial) or -3E (Extended)

Optional SRAM

Technology	QDR II+ 8M x 18 b4
Performance	1.8 GB/s simultaneous r/w per bank
Capacity	32 MB across two banks of 16 MB

Digital I/O

PCI Express Bus on Edge Fingers (PCI Express), P5 (XMC/CCXMC), P1 (VPX)	x8 or x4 electrical, Gen 2 backward compatible with Gen 1 and upward comaptible with Gen 3
General Purpose I/O (GPIO) on 15-pin Nano-D	6-bit LVTTL (3.3V), plus single 50 Ω or Hi-Z terminated LVTTL (3.3V / 5V tolerant) trigger
User I/O (UIO) on 68-pin D-Sub (PCI Express), P4 (XMC/CCXMC), P2 (VPX)	48-bit LVTTL (3.3V or 2.5V) or 24-bit LVDS, plus 12-bit LVTTL (3.3V or 2.5V), plus 2-bit LVTTL (voltage determined by 48-bit selection)
Trigger [1] (TRIG) on SMA	50 Ω, (3.3V / 5V tolerant) LVTTL

Analog I/O

Receiver (RX) on SMA	50 Ω, ADC input
Clock/Reference [1] (CLK/REF) on SMA	50 Ω, external sample clock or 10 MHz reference to internal sample clock

Power [2] (No SRAM / 32MB SRAM)

PCI Express [3]	3.3V = 27mW AC Coupled: 12V = 10.5W / 16.2W DC Coupled: 12V = 14.8W / 20.5W
XMC or CCXMC [3]	3.3V = 27mW, VPWR = 5.8W / 11.5W AC Coupled: 12V = 4.7W DC Coupled: 12V = 7.3W, -12V = 1.4W
VPX [3]	3.3V = 27mW AC Coupled: 12V = 10.5W / 16.2W DC Coupled: 12V = 13.2W / 18.9W, -12V = 1.4W

Environmental [4]

Storage Temperature	-55 °C to 125 °C
Operating Ambient Temperature	-30 °C to 85 °C
Typical Air Flow [5]	150 LFM
Max Heat Sink Temperature	95 °C

Clock/Reference (CLK/REF) Performance

Clock Frequency (Fs) Range	80 to 310 MHz
Internal Clock Phase Noise	-100 dBc/Hz (10 kHz offset)
Internal Reference Accuracy	10 MHz +/- 1 ppm
External Clock Amplitude	2 dBm (0.8 Vpp) to 5 dBm (1.1 Vpp)
External Reference Amplitude	7 dBm (1.5 Vpp) to 13.5 dBm (3.0 Vpp)

Receiver (RX) Performance (AC / DC Coupled)

1 dB Passband	1 to 150 MHz / DC to 200 MHz
3 dB Passband	0.1 to 400 MHz / DC to 450 MHz
Full Scale Input Amplitude	12.0 dBm (2.5 Vpp) / 4.0 dBm (1.0 Vpp)
SNR (20.17 MHz Input)	74.9 dB / 67.7 dB
SINAD (20.17 MHz Input)	74.8 dB / 67.6 dB
SFDR (20.17 MHz Input)	95 dBc / 93 dBc
Channel Isolation (100 MHz)	81 dB / 81 dB
Optional Lowpass Filter	5-pole Butterworth or Chebychev

Transmitter (TX) Performance (AC / DC Coupled)

DAC Interpolation Factor	2X (2Fs), 4X (4Fs), or 8X (8Fs)
Max Interpolated Rate (DACCLK)	2X: 1150 MHz, 4X: 1500 MHz, 8X: 1500 MHz
1 dB Passband	1 to DACCLK/3 MHz / DC to DACCLK/3 MHz
Full Scale Output Amplitude	-2.0 dBm (0.5 Vpp) / 4.0 dBm (1.0 Vpp)
Noise Spectral Density	-160 dBm/Hz / -148 dBm/Hz
SFDR (77.5 MHz Output)	85 dBc / 85 dBc
Sample Clock Feed Through	-82 dBm / -67 dBm
Channel Isolation (100 MHz)	>90 dB / >90 dB
Optional Lowpass Filter	5-pole Butterworth or Chebychev

Software

Driver (32-bit or 64-bit)	Windows 7/8/10, Linux
API & Demonstration Code	C (C++ compatible)

Single Piece Price [6]

XC7K160T-2I	$3,790 (No SRAM) / $4,790 (32 MB SRAM)
XC7K325T-2I	$4,550 (No SRAM) / $5,550 (32 MB SRAM)
XC7K410T-2I	$5,300 (No SRAM) / $6,300 (32 MB SRAM)
XC7K160T-3E	$4,070 (No SRAM) / $5,070 (32 MB SRAM)
XC7K325T-3E	$5,070 (No SRAM) / $6,070 (32 MB SRAM)
XC7K410T-3E	$6,070 (No SRAM) / $7,070 (32 MB SRAM)

Contact Information

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[1] The TRIG and CLK/REF inputs are mutually exclusive, either one must be selected as a build option.
[2] Voltage monitors attached to the primary supply inputs provide measurements accessible through the software API.
[3] Voltages that do not supply power are omitted. Values do not include power consumed by the application specific FPGA logic. FPGA power is drawn from the VPWR source on XMC/CCXMC units and 12V on all others. FPGA logic power will incur a 10% efficiency loss through voltage converters.
[4] Temperature monitors distributed across the board provide measurements accessible through the software API.
[5] Required air flow will depend on the power consumed by the FPGA which is application specific.
[6] Prices shown for PCI Express, XMC, and CCXMC form factors; add $2,000 for the VPX form factor.