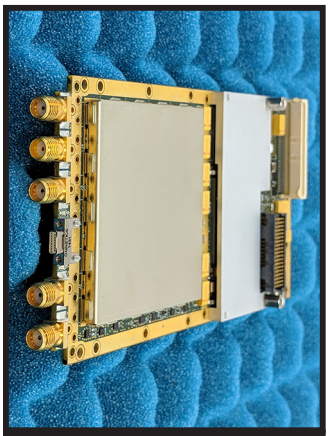
Red Rapids

SigStream™ RX4 16/250

Model 277


PCIe


XMC


CCXMC


VPX

The SigStream™ product family transforms a general purpose computer into a high speed signal acquisition/generation platform. The hardware incorporates a rich set of software programmable features that include selectable operating modes, external or timed event triggers, timestamped data samples, and flexible data formatting.

The Model 277 is designed around the Texas Instruments ADS42LB69 16-bit dual ADC. The 250 MHz sample clock is supplied by either the on-board frequency synthesizer or an external source. The frequency synthesizer can be phase locked to the local 10 MHz TCXO or an external reference can be used to achieve system-wide phase coherence.

Adopting open architecture hardware and software standards allows SigStream™ products to seamlessly transition from the desktop to embedded platforms.

Typical Applications

Spectrum monitor	Test & measurement
Radar & comms	Acqusition & telemetry
Signal recorder	Medical diagnostics
Software defined radio	Optical sensor interface

Four AC coupled 16-bit ADC channels

Internal or external sample clock (≤ 250 MHz)

Phase locked frequency synthesizer

Internal or external 10 MHz reference

Selectable triggers (HW, SW, TOD)

Continuous, snapshot, periodic operation

Available tuner with Fs/2^{23} resolution

Available programmable FIR filters

ANSI/VITA 49 compliant data format

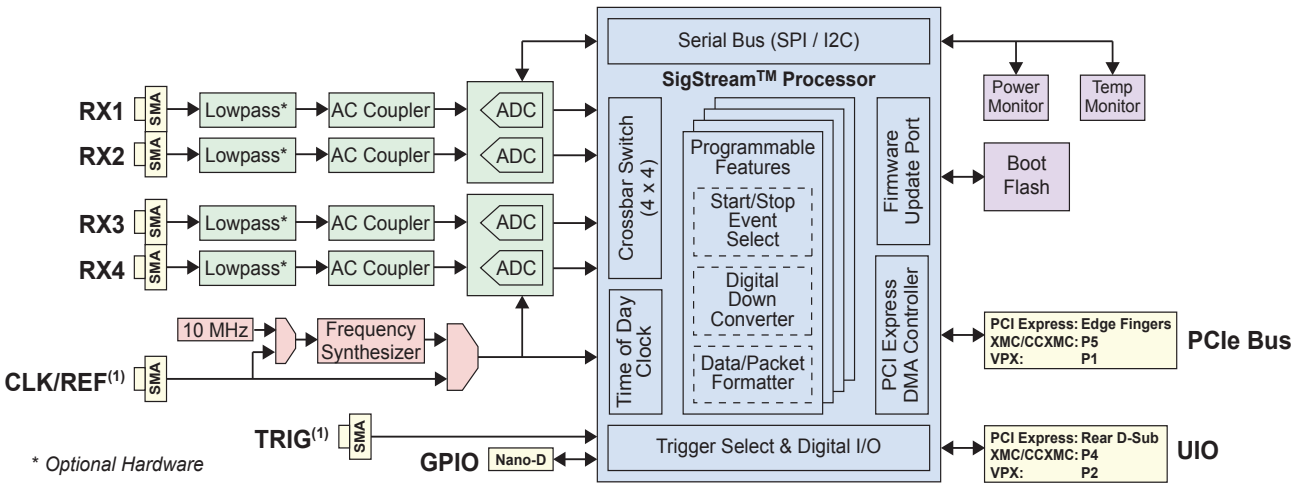
Temperature and power supply monitors

PCI Express (PCIe) x8 or x4 host bus

High performance scatter-gather DMA

Front and rear auxiliary connectors

Demostration software (C) with source



Form Factor

PCI Express (air cooled)	PCI Express 2.1, standard height, half-length, x8 or x4 physical edge connector
XMC (air cooled)	ANSI/VITA 42.0 single-width, ANSI/VITA 42.3
CCXMC (conduction cooled)	XMC plus ANSI/VITA 20
VPX (air or conduction cooled)	3U Eurocard, VITA 65, front panel I/O

Digital I/O

PCI Express Bus on Edge Fingers (PCI Express), P5 (XMC/CCXMC), P1 (VPX)	x8 or x4 electrical, Gen 2 backward compatible with Gen 1 and upward comaptible with Gen 3
General Purpose I/O (GPIO) on 15-pin Nano-D	50 Ω or Hi-Z terminated LVTTL (3.3V / 5V tolerant) trigger, plus 6-bits customized upon request
User I/O (UIO) on 68-pin D-Sub (PCI Express), P4 (XMC/CCXMC), P2 (VPX)	62-bits customized upon request
Trigger [1] (TRIG) on SMA	50 Ω, (3.3V / 5V tolerant) LVTTL

Analog I/O

Receiver (RX) on SMA	50 Ω, ADC input
Clock/Reference [1] (CLK/REF) on SMA	50 Ω, external sample clock or 10 MHz reference to internal sample clock

Power

PCI Express [4]	12V = 14.7W, 3.3V = 27mW
XMC or CCXMC [4]	12V = 2.3W, VPWR = 7.9W, 3.3V = 2.8W
VPX [4]	12V = 10.2W, 3.3V = 2.8W

Environmental

Storage Temperature	-55 °C to 125 °C
Operating Ambient Temperature	-30 °C to 85 °C
Typical Air Flow	150 LFM
Max Heat Sink Temperature	95 °C

Software

Driver (32-bit or 64-bit)	Windows 7/8/10, Linux
API & Demonstration Code	C (C++ compatible)

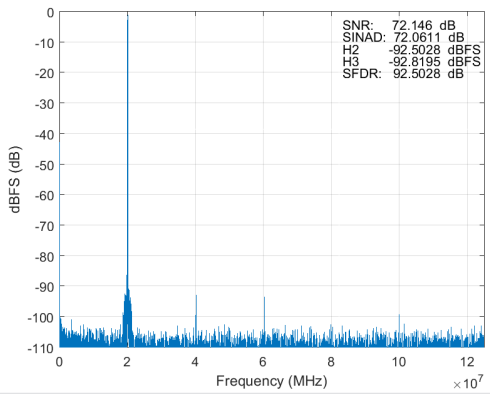
Clock/Reference (CLK/REF) Performance

Clock Frequency (Fs) Range	50 to 250 MHz
Internal Clock Phase Noise	-100 dBc/Hz (10 kHz offset)
Internal Reference Accuracy	10 MHz +/- 1 ppm
External Clock Amplitude	2 dBm (0.8 Vpp) to 13 dBm (2.8 Vpp)
External Reference Amplitude	7 dBm (1.5 Vpp) to 14.8 dBm (3.5 Vpp)

Receiver (RX) Performance

Passband	1 to 250 MHz (1 dB), 0.1 to 500 MHz (3 dB)
Full Scale Input Amplitude	10.8 dBm [2] (2.2 Vpp [2]), 12.8 dBm [3] (2.8 Vpp [3])
SNR (20.17 MHz Input)	73.5 dB [2], 74.8 dB [3]
SINAD (20.17 MHz Input)	73.4 dB [2], 74.7 dB [3]
SFDR (20.17 MHz Input)	90 dBc [2], 87 dBc [3]
Channel Isolation (50 MHz)	90 dB
Optional Lowpass Filter	5-pole Butterworth or Chebychev

Typical Performance Characteristics [2]



Start/Stop Events

Software Command	API function
External Trigger	SMA or GPIO connector input
Time of Day	ADC clock period fractional seconds resolution, seconds syncrhonized to external source (GPS, IRIG) or internal fractional seconds counter
Periodic Frame Length	≤ 2^{32} – 1 ADC clock periods
Sample/Cycle Count	≤ 2^{32} – 1 cycles
Scheduler	≤ 512 programmable time slots per frame

Default Digital Down Converter [5]

Real/Complex Samples	Bypass DDC to pass real (raw) ADC samples, DDC converts real samples to complex values
Tuner Resolution	Fs / 2^{23} (29.8 Hz @ Fs = 250 MHz)
Filter Stage #1	87-tap FIR, Fs (real) max input rate, Fs/2 (complex) max output rate, downsampler ≤ 2^{16} – 1
Filter Stage #2	127-tap FIR, Fs/2 (complex) max input/output rate, downsampler ≤ 2^{16} – 1
Filter Stage #3	255-tap FIR, Fs/4 (complex) max input/output rate, downsampler ≤ 2^{16} – 1

Data/Packet Formatter

Compliance Specification	ANSI/VITA 49
Data Item Size (bits)	4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 32
Item Packing Field Size (bits)	8, 10, 12, 14, 16, 20, 24, 32
Optional Event Tags	ADC over-range, trigger
Packet Options	Disabled, processing efficient, link efficient

Single Piece Price

PCI Express, XMC, CCXMC	$4,900
VPX	$6,900

Contact Information

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[1] Both the TRIG and CLK/REF inputs are available on the PCI Express form factor, all other form factors are limited to either one as a build option.
[2] Measurement with ADC programmed to default 2.0 Vpp full-scale input voltage range.
[3] Measurement with ADC programmed to maximum 2.5 Vpp full-scale input voltage range.
[4] Voltages available on the connector that do not supply power are omitted.
[5] All FIR filters are symmetric with programmable coefficients and can be individually bypassed. Custom architectures available upon request.

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