The SigStream™ product family transforms a general purpose computer into a high speed signal acquisition/generation platform. The hardware incorporates a rich set of software programmable features that include selectable operating modes, external or timed event triggers, timestamped data samples, and flexible data formatting.

The Model 277 is designed around the Texas Instruments ADS42LB69 16-bit dual ADC. The 250 MHz sample clock is supplied by either the on-board frequency synthesizer or an external source. The frequency synthesizer can be phase locked to the local 10 MHz TCXO or an external reference can be used to achieve system-wide phase coherence.

Adopting open architecture hardware and software standards allows SigStream™ products to seamlessly transition from the desktop to embedded platforms.

**Typical Applications**

- Spectrum monitor
- Radar & comms
- Signal recorder
- Software defined radio
- Test & measurement
- Acquisition & telemetry
- Medical diagnostics
- Optical sensor interface

Four AC coupled 16-bit ADC channels
Internal or external sample clock (≤ 250 MHz)
Phase locked frequency synthesizer
Internal or external 10 MHz reference
Selectable triggers (HW, SW, TOD)
Continuous, snapshot, periodic operation
Available tuner with Fs/2²³ resolution
Available programmable FIR filters
ANSI/VITA 49 compliant data format
Temperature and power supply monitors
PCI Express (PCIe) x8 or x4 host bus
High performance scatter-gather DMA
Front and rear auxiliary connectors
Demostration software (C) with source

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* Optional Hardware

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PCI Express: Edge Fingers XMC/CCXMC; P5
VPX: P1

PCI Express: Rear D-Sub XMC/CCXMC; P4
VPX: P2

PCI Express: Rear Nano-D
UIO

**SigStream™ RX4 16/250**

**Model 277**
**Form Factor**

PCI Express (air cooled)  
XMC (air cooled)  
CCXMC (conduction cooled)  
VPX (air or conduction cooled)  

**Digital I/O**

PCI Express Bus on Edge Fingers (PCI Express), P5 (XMC/CCXMC), P1 (VPX)  
General Purpose I/O (GPIO) on 15-pin Nano-D  
User I/O (UIO) on 68-pin D-Sub (PCI Express), P4 (XMC/CCXMC), P2 (VPX)  
Trigger (TRIG) on SMA  

**Analog I/O**

Receiver (RX) on SMA  
Clock/Reference (CLK/REF) on SMA  

**Power**

PCI Express  
XMC or CCXMC  
VPX  

**Environmental**

Storage Temperature  
Operating Ambient Temperature  
Typical Air Flow  
Max Heat Sink Temperature  

**Software**

Driver (32-bit or 64-bit)  
API & Demonstration Code  

**Clock/Reference (CLK/REF) Performance**

Clock Frequency (Fs) Range  
Internal Clock Phase Noise  
Internal Reference Accuracy  
External Clock Amplitude  
External Reference Amplitude  

**Receiver (RX) Performance**

Passband  
Full Scale Input Amplitude  
SNR (20.17 MHz Input)  
 SINAD (20.17 MHz Input)  
SFDR (20.17 MHz Input)  
Channel Isolation (50 MHz Input)  
Optional Lowpass Filter  

**Typical Performance Characteristics**

- **Start/Stop Events**
  - Software Command: API function
  - External Trigger: SMA or GPIO connector input
  - Time of Day: ADC clock period fractional seconds resolution, seconds synchronized to external source (GPS, IRIG) or internal fractional seconds counter
  - Periodic Frame Length: \( \leq 2^{15} - 1 \) ADC clock periods
  - Sample/Cycle Count: \( \leq 2^{29} - 1 \) cycles
  - Scheduler: \( \leq 512 \) programmable time slots per frame

- **Default Digital Down Converter**
  - Real/Complex Samples: Bypass DDC to pass raw (raw) ADC samples, DDC converts real samples to complex values
  - Tuner Resolution: \( Fs / 2^{23} \) (29.8 Hz @ \( Fs = 250 \text{ MHz} \))
  - Filter Stage #1: 87-tap FIR, Fs (real) max input rate, Fs/2 (complex) max output rate, downsampler \( \leq 2^{15} - 1 \)
  - Filter Stage #2: 127-tap FIR, Fs/2 (complex) max input/output rate, downsampler \( \leq 2^{15} - 1 \)
  - Filter Stage #3: 255-tap FIR, Fs/4 (complex) max input/output rate, downsampler \( \leq 2^{15} - 1 \)

- **Data/Packet Formatter**
  - Compliance Specification: ANSI/VITA 49
  - Data Item Size (bits): 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 32
  - Item Optional Tags: ADC over-range, trigger
  - Packet Options: Disabled, processing efficient, link efficient

- **Single Piece Price**
  - PCI Express, XMC, CCXMC: $4,700
  - VPX: $6,700

**Contact Information**

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(1) Both the TRIG and CLK/REF inputs are available on the PCI Express form factor, all other form factors are limited to either one as a build option.
(2) Measurement with ADC programmed to default 2.0 Vpp full-scale input voltage range.
(3) Measurement with ADC programmed to maximum 2.5 Vpp full-scale input voltage range.
(4) Voltages available on the connector that do not supply power are omitted.
(5) All FIR filters are symmetric with programmable coefficients and can be individually bypassed. Custom architectures available upon request.