The SigStream™ product family transforms a general purpose computer into a high speed signal acquisition/generation platform. The hardware incorporates a rich set of software programmable features that include selectable operating modes, external or timed event triggers, timestamped data samples, and flexible data formatting.

The Model 276 is designed around the Texas Instruments AD12D1600 12-bit dual ADC. The 1.5 GHz sample clock is supplied by either the on-board frequency synthesizer or an external source. The frequency synthesizer can be phase locked to the local 10 MHz TCXO or an external reference can be used to achieve system-wide phase coherence.

Adopting open architecture hardware and software standards allows SigStream™ products to seamlessly transition from the desktop to embedded platforms.

**Typical Applications**

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<th>Spectrum monitor</th>
<th>Test &amp; measurement</th>
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<td>Radar &amp; comms</td>
<td>Acquisition &amp; telemetry</td>
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<td>Software defined radio</td>
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</table>

Two AC or DC coupled 12-bit ADC channels

Internal or external sample clock (≤ 1.6 GHz)

Phase locked frequency synthesizer

Internal or external 10 MHz reference

Selectable triggers (HW, SW, TOD)

Continuous, snapshot, periodic operation

ANSI/VITA 49 compliant data format

Temperature and power supply monitors

PCI Express (PCIe) x8 or x4 host bus

High performance scatter-gather DMA

Front and rear auxiliary connectors

Demostration software (C) with source
**Form Factor**

- **PCI Express (air cooled)**: PCI Express 2.1, standard height, half-length, x8 or x4 physical edge connector
- **XMC (air cooled)**: ANSI/VITA 42.0 single-width, ANSI/VITA 42.3
- **CCXMC (conduction cooled)**: XMC plus ANSI/VITA 20
- **VPX (air or conduction cooled)**: 3U Eurocard, VITA 65, front panel I/O

**Digital I/O**

- **PCI Express Bus on Edge Fingers (PCI Express), PS (XMC/CCXMC), P1 (VPX)**: x8 or x4 electrical, Gen 2 backward compatible with Gen 1 and upward compatible with Gen 3
- **General Purpose I/O (GPIO) on 15-pin Nano-D**: 50 Ω or Hi-Z terminated LVTTL (3.3V / 5V tolerant) trigger, plus 6-bits customized upon request
- **User I/O (UIO) on 68-pin D-Sub (PCI Express), P4 (XMC/CCXMC), P2 (VPX)**: 62-bits customized upon request
- **Trigger**(1) (TRIG) on SMA: 50 Ω, (3.3V / 5V tolerant) LV TTL

**Analog I/O**

- **Receiver (RX) on SMA**: 50 Ω, ADC input
- **Clock/Reference (CLK/REF) on SMA**: 50 Ω, external sample clock or 10 MHz reference to internal sample clock

**Power**

- **PCI Express**(1)****: 12V = 13.9W
  - AC Coupled: 3.3V = 172mW
  - DC Coupled: 3.3V = 733mW
- **XMC or CCXMC**(1)****: 12V = 2.6W, VPWR = 11.2W
  - AC Coupled: 3.3V = 172mW
  - DC Coupled: 3.3V = 733mW
- **VPX**(1)****: 12V = 13.9W
  - AC Coupled: 3.3V = 172mW
  - DC Coupled: 3.3V = 733mW

**Environmental**

- **Storage Temperature**: -55 °C to 125 °C
- **Operating Ambient Temperature**: -30 °C to 85 °C
- **Typical Air Flow**: 150 LFM
- **Max Heat Sink Temperature**: 95 °C

**Clock/Reference (CLK/REF) Performance**

- **Clock Frequency (Fs) Range**: 150 to 1600 MHz
- **Internal Clock Phase Noise**: -100 dBc/Hz (10 kHz offset)
- **Internal Reference Accuracy**: 10 MHz +/- 1 ppm
- **External Clock Amplitude**: 4 dBm (1.0 Vpp) to 10 dBm (2.0 Vpp)
- **External Reference Amplitude**: 7 dBm (1.5 Vpp) to 13.5 dBm (3.0 Vpp)

**Receiver (RX) Performance (AC / DC Coupled)**

- **1 dB Passband**: 10 to 1000 MHz / DC to 1000 MHz
- **3 dB Passband**: 0.1 to 2500 MHz / DC to 1100 MHz
- **Full Scale Input Amplitude (500 MHz Input)**: 3.3 dBm (0.93 Vpp) / 2.1 dBm (0.81 Vpp)
- **SNR (124.8 MHz Input)**: 56.0 dB / 52.6 dB
- **SINAD (124.8 MHz Input)**: 54.7 dB / 52.4 dB
- **SFDR (124.8 MHz Input)**: 62.5 dBc / 66.0 dBc
- **Channel Isolation (500 MHz)**: 58 dB / 47 dB
- **Optional Lowpass Filter**: 5-pole Butterworth or Chebychev

**Typical Performance Characteristics**

- **Start/Stop Events**
  - **Software Command**: API function
  - **External Trigger**: SMA or GPIO connector input
  - **Time of Day**: ADC clock period fractional seconds resolution, seconds synchronized to external source (GPS, IRIG) or internal fractional seconds counter
  - **Periodic Frame Length**: ≤ 2^32 – 1 ADC clock periods
  - **Sample/Cycle Count**: ≤ 2^32 – 1 cycles
  - **Scheduler**: ≤ 512 programmable time slots per frame

- **Real Resampler**
  - **Downsample Ratio**: 1 to ≤ 2^16 – 1

- **Data/Packet Formatter**
  - **Compliance Specification**: ANSI/VITA 49
  - **Data Item Size (bits)**: 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 32
  - **Item Packing Field Size (bits)**: 8, 10, 12, 16
  - **Optional Event Tags**: ADC over-range, trigger
  - **Packet Options**: Disabled, processing efficient, link efficient

- **Software**
  - **Driver**: (32-bit or 64-bit) Windows 7/8/10, Linux
  - **API & Demonstration Code**: C (C++ compatible)

- **Single Piece Price**
  - **PCI Express, XMC, CCXMC**: $6,990
  - **VPX**: $8,990

**Contact Information**

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(1) Voltages available on the connector that do not supply power are omitted.