The SigStream™ product family transforms a general purpose computer into a high speed signal acquisition/generation platform. The hardware incorporates a rich set of software programmable features that include selectable operating modes, external or timed event triggers, timestamped data samples, and flexible data formatting.

The Model 273 is designed around the Analog Devices AD9652 16-bit dual ADC. The 310 MHz sample clock is supplied by either the on-board frequency synthesizer or an external source. The frequency synthesizer can be phase locked to the local 10 MHz TCXO or an external reference can be used to achieve system-wide phase coherence.

Adopting open architecture hardware and software standards allows SigStream™ products to seamlessly transition from the desktop to embedded platforms.

**Typical Applications**

- Spectrum monitor
- Radar & comms
- Signal recorder
- Software defined radio
- Test & measurement
- Acquisition & telemetry
- Medical diagnostics
- Optical sensor interface

Two AC or DC coupled 16-bit ADC channels
- Internal or external sample clock (≤ 310 MHz)
- Phase locked frequency synthesizer
- Internal or external 10 MHz reference
- Selectable triggers (HW, SW, TOD)
- Continuous, snapshot, periodic operation
- Available tuner with Fs/2^{23} resolution
- Available programmable FIR filters
- ANSI/VITA 49 compliant data format
- Temperature and power supply monitors
- PCI Express (PCIe) x8 or x4 host bus
- High performance scatter-gather DMA
- Front and rear auxiliary connectors
- Demostration software (C) with source code
Form Factor
- PCI Express (air cooled): PCI Express 2.1, standard height, half-length, x8 or x4 physical edge connector
- XMC (air cooled): ANSI/VITA 42.0 single-width, ANSI/VITA 42.3
- CCXMC (conduction cooled): XMC plus ANSI/VITA 20
- VPX (air or conduction cooled): 3U Eurocard, VITA 65, front panel I/O

Digital I/O
- PCI Express Bus on Edge Fingers (PCI Express), P5 (XMC/CCXMC), P1 (VPX): x8 or x4 electrical, Gen 2 backward compatible with Gen 1 and upward compatible with Gen 3
- General Purpose I/O (GPIO) on 15-pin Nano-D: 50 Ω or Hi-Z terminated LVTTTL (3.3V / 5V tolerant) trigger, plus 6-bits customized upon request
- User I/O (UIO) on 68-pin D-Sub (PCI Express), P4 (XMC/CCXMC), P2 (VPX): 62-bits customized upon request
- Trigger (TRIG) on SMA: 50 Ω, (3.3V / 5V tolerant) LVTTTL

Analog I/O
- Receiver (RX) on SMA: 50 Ω, ADC input
- Clock/Reference (CLK/REF) on SMA: 50 Ω, external sample clock or 10 MHz reference to internal sample clock

Power
- PCI Express (1): AC Coupled: 12V = 10.8W, 3.3V = 27mW. DC Coupled: 12V = 12.7W, 3.3V = 32mW
- XMC or CCXMC (1): VPWR = 7.1W, 3.3V = 27mW. AC Coupled: 12V = 4.7W. DC Coupled: 12V = 7.3mW, -12V = 1.4W
- VPX (1): 3.3V = 27mW. AC Coupled: 12V = 10.8W. DC Coupled: 12V = 12.0W, -12V = 1.4W

Environmental
- Storage Temperature: -55 °C to 125 °C
- Operating Ambient Temperature: -30 °C to 85 °C
- Typical Air Flow: 150 LFM
- Max Heat Sink Temperature: 95 °C

Software
- Driver (32-bit or 64-bit): Windows 7/8/10, Linux
- API & Demonstration Code: C (C++ compatible)

Clock/Reference (CLK/REF) Performance
- Clock Frequency (Fs) Range: 80 to 310 MHz
- Internal Clock Phase Noise: -100 dB/Hz (10 kHz offset)
- Internal Reference Accuracy: 10 MHz +/- 1 ppm
- External Clock Amplitude: 2 dBm (0.8 Vpp) to 5 dBm (1.1 Vpp)
- External Reference Amplitude: 7 dBm (1.5 Vpp) to 13.5 dBm (3.0 Vpp)

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Typical Performance Characteristics (2)
Receiver (RX) Performance (AC / DC Coupled)
- 1 dB Passband: 1 to 150 MHz / DC to 200 MHz
- 3 dB Passband: 0.1 to 400 MHz / DC to 450 MHz
- Full Scale Input Amplitude: 12.0 dBm (2.5 Vpp) / 4.0 dBm (1.0 Vpp)
- SNR (20.17 MHz Input): 74.9 dB / 67.7 dB
- SINAD (20.17 MHz Input): 74.8 dB / 67.6 dB
- SFDR (20.17 MHz Input): 95 dBc / 93 dBc
- Channel Isolation (100 MHz): 81 dB / 81 dB
- Optional Lowpass Filter: 5-pole Butterworth or Chebychev

Start/Stop Events
- Software Command: API function
- External Trigger: SMA or GPIO connector input
- Time of Day: ADC clock period fractional seconds resolution, seconds synchronized to external source (GPS, IRIG) or internal fractional seconds counter
- Periodic Frame Length: ≤ 232 – 1 ADC clock periods
- Sample/Cycle Count: ≤ 232 – 1 cycles
- Scheduler: ≤ 512 programmable time slots per frame

Default Digital Down Converter (2)
- Real/Complex Samples: Bypass DDC to pass real (raw) ADC samples, DDC converts real samples to complex values
- Tuner Resolution: Fs / 233 (37.0 Hz @ Fs = 310 MHz)
- Filter Stage #1: 87-tap FIR, Fs (real) max input rate, Fs/2 (complex) max output rate, downsampler ≤ 216 – 1
- Filter Stage #2: 127-tap FIR, Fs/2 (complex) max input/output rate, downsampler ≤ 216 – 1
- Filter Stage #3: 255-tap FIR, Fs/4 (complex) max input/output rate, downsampler ≤ 216 – 1

Data/Packet Formatter
- Compliance Specification: ANSI/VITA 49
- Data Item Size (bits): 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 32
- Item Packing Size (bits): 8, 10, 12, 14, 16, 20, 24, 32
- Optional Event Tags: ADC over-range, trigger
- Packet Options: Disabled, processing efficient, link efficient

Single Piece Price
- PCI Express, XMC, CCXMC: $3,700
- VPX: $5,700

(1) Voltages available on the connector that do not supply power are omitted.
(2) All FIR filters are symmetric with programmable coefficients and can be individually bypassed. Custom architectures available upon request.

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