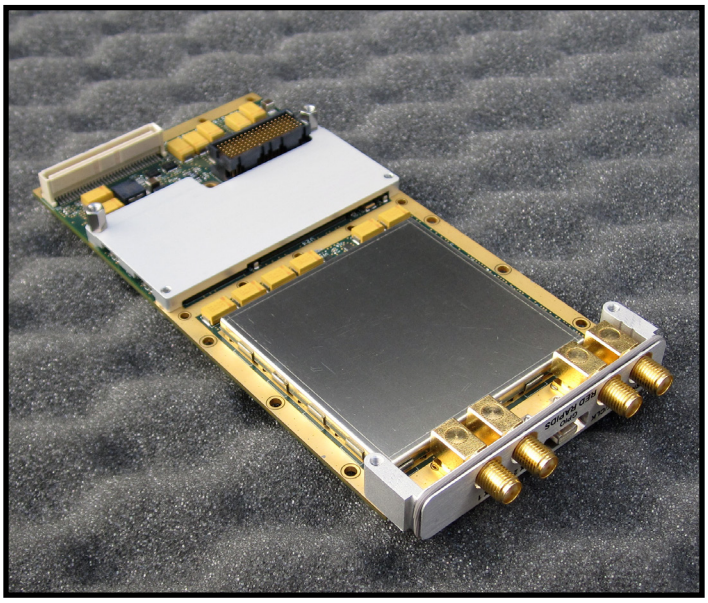
Red Rapids

SigStream RX2 16/310

Model 273



- **Available in XMC, CCXMC, PCIe formats**
- **Dual 16-bit (310 MHz) ADCs**
- **AC or DC coupled analog inputs**
- **Fixed or variable frequency synthesizer**
- **Selectable triggers (HW, SW, TOD)**
- **Continuous, snapshot, periodic operation**
- **37 Hz tuning resolution (Fs = 310 MHz)**
- **Full bandwidth plus ten octave sub-bands**
- **VITA 49 compliant data packet format**
- **PCI Express (PCIe) x8 Gen 2 bus**
- **Scatter-gather DMA bus master**
- **Windows, Linux, VxWorks drivers & API**

Signal Acquisition

The *SigStream* product family performs general purpose signal acquisition for a broad range of applications (scientific, medical, industrial, communications). The Model 273 can supply either raw ADC samples or complex samples produced by the embedded digital down converter. The down converter features a tuning resolution of $Fs/2^{23}$ and ten selectable octave sub-bands in addition to the full output bandwidth of the ADC.

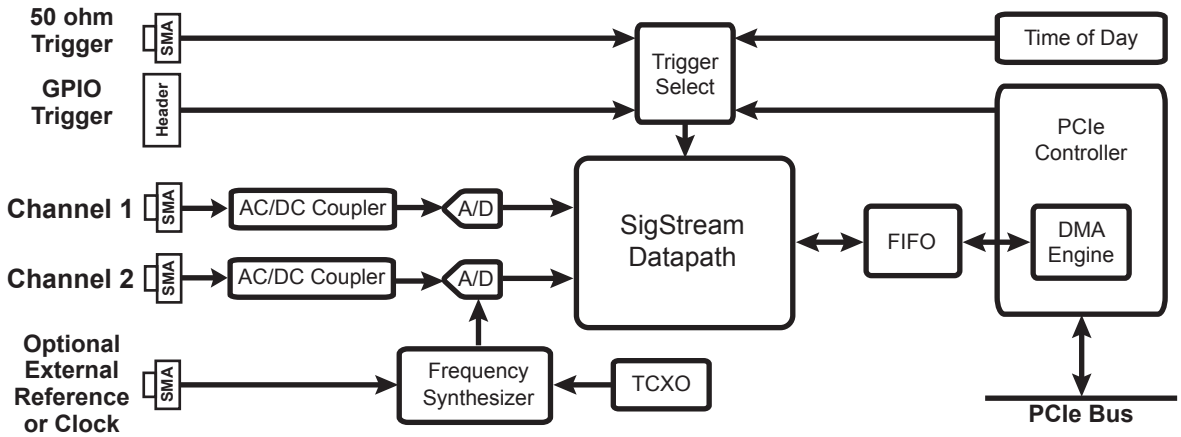
The Model 273 is designed around the Analog Devices AD9652 16-bit ADC. The 310 MHz sample clock is supplied by either the on-board frequency synthesizer or an external source. The frequency synthesizer can be phase locked to the local 10 MHz TCXO or an external reference can be used to achieve system-wide phase coherence.

The on-board frequency synthesizer can be fixed to a specified sample rate for optimum phase noise and spurious performance, or it can be variable for maximum flexibility. The variable frequency synthesizer is programmed in 100 kHz step sizes.

The Model 273 is available as a PCI Express mezzanine card (XMC), conduction cooled mezzanine card (CCXMC), or half-length PCI Express (PCIe) adapter card. The CCXMC can be mounted to any VITA 20-2001 compliant host without modification. All form factors offer four lane (x4) or eight lane (x8) bus operation at Gen 2 performance.

All *SigStream* products include a rich set of software programmable features that include selectable operating modes (continuous, snapshot, periodic), external or timed event triggers, timestamped data samples, data sizing, and data packing. Data is sent to the host computer as a continuous stream of samples or in data packets defined by the VITA 49 specification.

Signal acquisition can be started by software command, software trigger, external hardware trigger, or preset time of day. These same options are available to stop a collection.



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The start/stop events can be used to define the length of a snapshot, but there is also a feature to simply specify the number of samples to process following the start event.

The *SigStream* product can be programmed to repeat snapshots on a periodic interval. The length of each cycle is defined by the start/stop events described above, or a fixed length frame duration. Periodic operation is terminated by software command, preset time of day, or simply specifying the number of cycles to process.

A GPIO header provides separate hardware trigger connections for each channel. The trigger source used by each datapath is software selectable. A 50 ohm terminated coaxial input offers a second trigger source that provides controlled impedance through the cable interconnect. The coaxial trigger is standard on the two channel configuration (RX2

The Model 273 monitors both power consumption and temperature during normal operation. Current measurements are available on all of the primary voltage supplies. Temperature sensors monitor the DSP die temperature, ADC die temperature, and four other locations on the card.

A DMA engine assigned to each channel manages data transfers between the PCIe controller and host memory. The DMA engine allows the receiver to automatically initiate a PCIe burst transaction when data needs to be transferred. High performance DMA techniques are supported by both the hardware and software to optimize data transfer efficiency. Memory fragmentation problems are eliminated by supporting thousands of scatter-gather DMA buffers in host memory.

The progress of DMA transfers is tracked by polling the hardware or monitoring interrupts. The spacing of interrupts is variable, they are programmed to fire when the desired number of DMA pages are refreshed. The *SigStream* product includes an interrupt timer function to measure the response time of the host. This is used to establish an optimum interrupt frequency that will not overwhelm the software.

Demonstration software is provided with the hardware to quickly establish a path to end-user application code. The API is supported with drivers for Windows™, Linux, or VxWorks operating systems.

Typical Applications

- **Multi-channel signal acquisition**
- **High speed instrumentation**
- **Signal intelligence (SIGINT) collection**
- **Software defined radio**
- **Signal recorder**

Specification Summary

Receiver Performance

Measured characteristics:
- Full power (3 dB) bandwidth: 450 MHz
- SNR: 74 dB (First Nyquist typical)
- SFDR: 89 dBc (First Nyquist typical)
- Channel isolation: 90 dB (typical)

Phase noise: -100 dBc/Hz (10 kHz offset)
Internal reference: 10 MHz +/- 1.0 ppm

Digital Down Converter

37 Hz tuning resolution (Fs = 310 MHz)
Full Nyquist output bandwidth (BW)
Octave sub-bands ($BW/2^N$, N = 1 to 10)

Hardware

Format: XMC, CCXMC, half-length PCIe
PCIe: x4 or x8 Gen 2
GPIO: 6-bit LVTTL or 3-bit LVDS
Selectable internal or external sample clock
Selectable internal or external reference
Coaxial trigger (50 ohm terminated)
GPIO triggers (50 ohm terminated option)
Power dissipation: 15 Watts

Software

Adapter driver: Linux, Windows, VxWorks
SigStream application example

Build Options

Synthesizer frequency:
- 310 MHz (Maximum ADC specification)
- 213.33 MHz (160 MHz IF sampling)
- Programmable (Degraded phase noise)

Conformal coat for harsh environments

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