# **Red Rapids**

# SigStream<sup>™</sup> XCVR2 16/250 Model 272





The SigStream<sup>™</sup> product family transforms a general purpose computer into a high speed signal acquisition/generation platform. The hardware incorporates a rich set of software programmable features that include selectable operating modes, external or timed event triggers, timestamped data samples, and flexible data formatting.

The Model 272 is designed around the Analog Devices AD9652 16-bit dual ADC and AD9142A DAC. The 250 MHz sample clock is supplied by either the on-board frequency synthesizer or an external source. The frequency synthesizer can be phase locked to the local 10 MHz TCXO or an external reference can be used to achieve system-wide phase coherence.

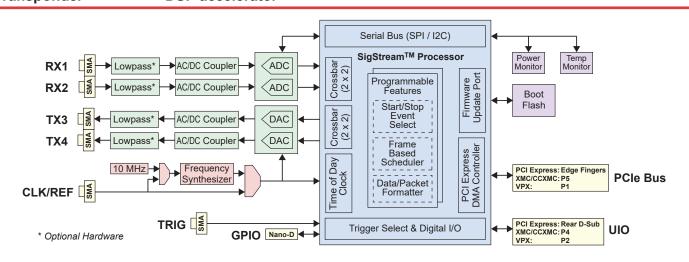
Adopting open architecture hardware and software standards allows SigStream<sup>™</sup> products to seamlessly transition from the desktop to embedded platforms.

# **Typical Applications**

Radar & commsTest & measurementSignal record/playbackAcquisition & telemetrySoftware defined radioMedical diagnosticsTransponderDSP accelerator



Two AC or DC coupled 16-bit ADC channels Two AC or DC coupled 16-bit DAC channels Internal or external sample clock (≤ 250 MHz) Phase locked frequency synthesizer Internal or external 10 MHz reference Selectable triggers (HW, SW, TOD) Continuous, snapshot, periodic operation ANSI/VITA 49 compliant data format Temperature and power supply monitors PCI Express (PCIe) x8 or x4 host bus High performance scatter-gather DMA Front and rear auxiliary connectors Demostration software (C) with source



# **Form Factor**

PCI Express (air cooled)	PCI Express 2.1, standard height, half-length, x8 or larger physical edge connector
XMC (air cooled)	ANSI/VITA 42.0 single-width, ANSI/VITA 42.3
CCXMC (conduction cooled)	XMC plus ANSI/VITA 20
VPX (air or conduction cooled)	3U Eurocard, VITA 65, front panel I/O

# **Digital I/O**

PCI Express Bus on Edge Fingers (PCI Express), P5 (XMC/CCXMC), P1 (VPX)	x8 or x4 electrical, Gen 2 backward compatible with Gen 1 and upward comaptible with Gen 3
General Purpose I/O (GPIO) on 15-pin Nano-D	50 $\Omega$ or Hi-Z terminated LVTTL (3.3V / 5V tolerant) trigger, plus 6-bits customized upon request
User I/O (UIO) on 68-pin D-Sub (PCI Express), P4 (XMC/CCXMC), P2 (VPX)	62-bits customized upon request
Trigger <sup>(1)</sup> (TRIG) on SMA	50 $\Omega,$ (3.3V / 5V tolerant) LVTTL

# Analog I/O

Receiver (RX) on SMA	50 Ω, ADC input
Transmitter (TX) on SMA	50 Ω, DAC output
Clock/Reference <sup>(1)</sup> (CLK/REF) on SMA	50 $\Omega_{\!\!,}$ external sample clock or 10 MHz reference to internal sample clock

#### Power

PCI Express <sup>(2)</sup>	3.3V = 27mW AC Coupled: 12V = 14.1W DC Coupled: 12V = 18.4W
XMC or CCXMC <sup>(2)</sup>	3.3V = 27mW, VPWR = 9.4W AC Coupled: 12V = 4.7W DC Coupled: 12V = 7.3W, -12V = 1.4W
VPX <sup>(2)</sup>	3.3V = 27mW AC Coupled: 12V = 14.1W DC Coupled: 12V = 16.8W, -12V = 1.4W

#### **Environmental**<sup>(4)</sup>

Storage Temperature	-55 °C to 125 °C
Operating Ambient Temperature	-30 °C to 85 °C
Typical Air Flow	150 LFM
Max Heat Sink Temperature	95 °C

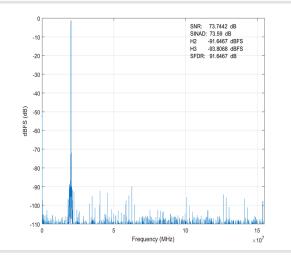
# **Start/Stop Events**

Software Command	API function
External Trigger	SMA or GPIO connector input
Time of Day	ADC clock period fractional seconds resolution, seconds syncrhonized to external source (GPS, IRIG) or internal fractional seconds counter
Periodic Frame Length	$\leq 2^{32} - 1$ ADC clock periods
Sample/Cycle Count	$\leq 2^{32} - 1$ cycles
Scheduler	≤ 512 programmable time slots per frame

# **Clock/Reference (CLK/REF) Performance**

Clock Frequency (Fs) Range	80 to 250 MHz	Address
Internal Clock Phase Noise	-100 dBc/Hz (10 kHz offset)	
Internal Reference Accuracy	10 MHz +/- 1 ppm	Phone

# **Typical RX Performance Characteristics**



#### **Receiver (RX) Performance (AC / DC Coupled)**

1 dB Passband	1 to 150 MHz / DC to 200 MHz
3 dB Passband	0.1 to 400 MHz / DC to 450 MHz
Full Scale Input Amplitude	12.0 dBm (2.5 Vpp) / 4.0 dBm (1.0 Vpp)
SNR (20.17 MHz Input)	74.9 dB / 67.7 dB
SINAD (20.17 MHz Input)	74.8 dB / 67.6 dB
SFDR (20.17 MHz Input)	95 dBc / 93 dBc
Channel Isolation (100 MHz)	81 dB / 81 dB
Optional Lowpass Filter	5-pole Butterworth or Chebychev

#### Transmitter (TX) Performance (AC / DC Coupled)

DAC Interpolation Factor	2X (2Fs), 4X (4Fs), or 8X (8Fs)
Max Interpolated Rate (DACCLK)	2X: 1150 MHz, 4X: 1500 MHz, 8X: 1500 MHz
1 dB Passband	1 to DACCLK/3 MHz / DC to DACCLK/3 MHz
Full Scale Output Amplitude	-2.0 dBm (0.5 Vpp) / 4.0 dBm (1.0 Vpp)
Noise Spectral Density	-160 dBm/Hz / -148 dBm/Hz
SFDR (77.5 MHz Output)	85 dBc / 85 dBc
Sample Clock Feed Through	-82 dBm / -67 dBm
Channel Isolation (100 MHz)	>90 dB / >90 dB
Optional Lowpass Filter	5-pole Butterworth or Chebychev

#### Software

Driver (32-bit or 64-bit)	Windows 8/10, Linux
API & Demonstration Code	C (C++ compatible)

#### **Single Piece Price**

PCI Express, XMC, CCXMC	\$3,990
VPX	\$5,990

#### **Contact Information**

Address	Red Rapids 797 N Grove Rd, Suite 101 Richardson, TX 75081
Phone	972-671-9570 (+1 country code)

<sup>(1)</sup> The TRIG and CLK/REF inputs are mutually exclusive, either one must be selected as a build option. <sup>(2)</sup> Voltages available on the connector that do not supply power are omitted. voltage converters.

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